LAMPIRAN A

LAMPIRAN A

Penurunan Persamaan Penguat Instrumentasi

Penguat EKG pada prinsipnya adalah penguat differensial dengan *buffer* pada kedua masukannya, sehingga penurunan persamaan penguatan penguat instrumentasi dapat dibagi kedalam dua bagian yang berdiri sendiri yaitu bagian penguat differensial dan bagian *buffer* (Aston, 1990)

Berikut ini penurunan persamaan penguat pada bagian *buffer*. Diasumsikan penguat operasional ideal sehingga tidak ada arus yang mengalir ke dalam terminal input.. Sehingga arus yang mengalir melalui Ro sama dengan arus yang mengalir melalui Ro dan R1 dan R2 jadi (Aston, 1990):

$$V_3 = V_{i1}$$

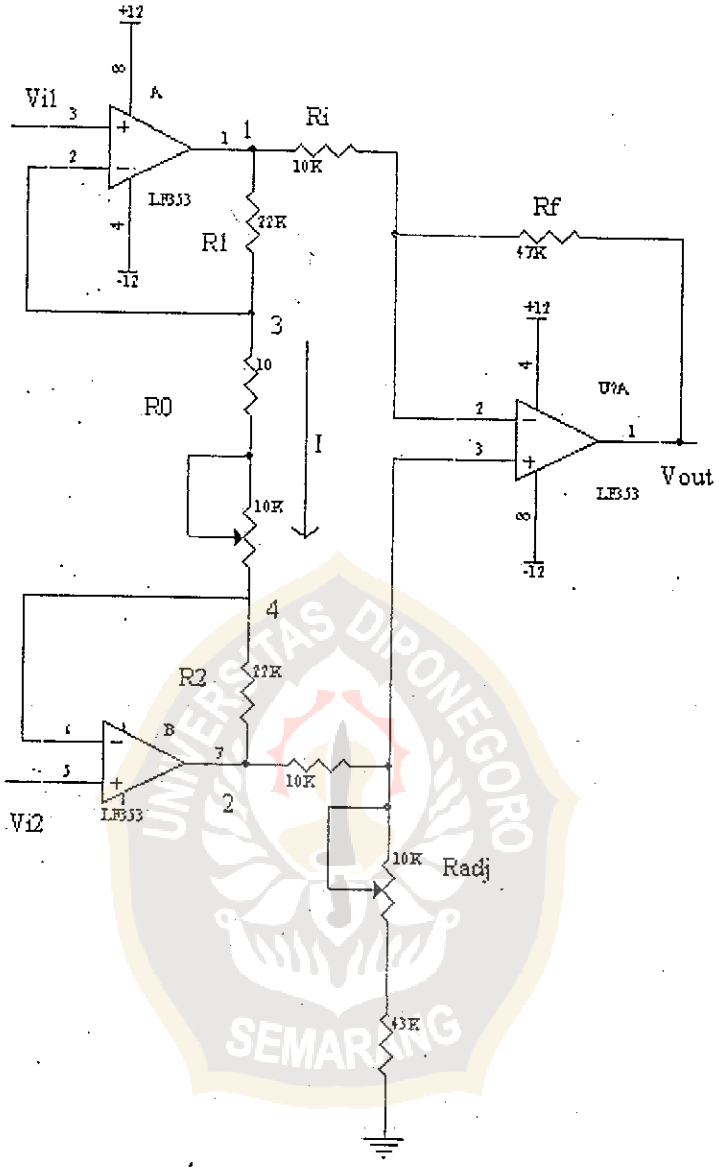
dan

$$V_4 = V_{i2}$$

$$\frac{V_3 - V_4}{R_0} = \frac{V_1 - V_2}{R_1 + R_2 + R_0}$$

$$V_1 - V_2 = \frac{R_1 + R_2 + R_0}{R_0}(V_{i1} - V_{i2}) \qquad \text{(A.1)}$$

Dari persamaan dapat dilihat bahwa penguatan sinyal oleh bagian *buffer* adalah sebesar $(R_1+R_2+R_0)/R_0$.



Gambar A.1 Penguat Instrumentasi

Untuk menurunkan bagian differensial amplifier harus mengacu kepada penurunan persamaan penguatan penguat *inverting* dan penguat *non-inverting* karena penguat diferensial pada dasarnya merupakan gabungan kedua penguat

tersebut. Berikut ini penurunan persamaan penguatan penguat *inverting* dan penguat *non-inverting*.

Penurunan persamaan penguatan penguat *inverting*. Penguat operasional dikatakan ideal jika $E_d = 0$ sehingga $V_d = 0$ (Boylestad, 1992).

$$I = \frac{V_i}{R_i}$$

$$V_{Rf} = R_f . I$$

$$V_{Rf} = R_f \frac{V_i}{R_i}$$

$$V_{Rf} = \frac{R_f}{R_i} V_i$$

$$V_o = V_{BO}$$

$$V_{Rf} = V_{AB}$$

$$V_{Rf} = V_{OB}$$

$$V_{Rf} = -V_{BO}$$

karena

$$V_o = -V_{BO}$$

dan

$$V_o = -V_{Rf}$$

maka

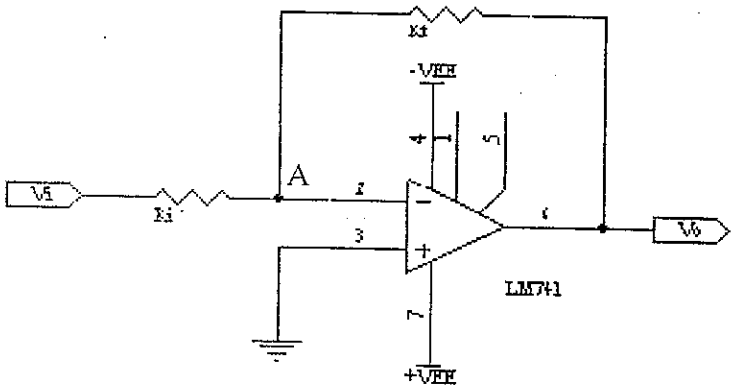
$$V_o = -V_{Rf}$$

$$\therefore V_o = -\frac{R_f}{R_i} V_i$$

sehingga

$$A_{CL} = \frac{V_o}{V_i}$$

$$A_{CL} = -\frac{R_f}{R_i} \qquad \text{(A.2)}$$



Gambar A.2 Penguat Inverting

Penurunan persamaan penguatan penguat *non-inverting*. Penguat operasional dikatakan ideal jika $E_d = 0$ sehingga $V_A = V_I$ (Boylestad, 1992).

$$I = \frac{V_i}{R_i}$$

$$V_{Rf} = R_f . I$$

$$V_{Rf} = R_f \frac{V_i}{R_i}$$

$$V_{Rf} = \frac{R_f}{R_i} V_i$$

$$V_o = V_{BO}$$

$$V_o = V_{Rf} + V_A$$

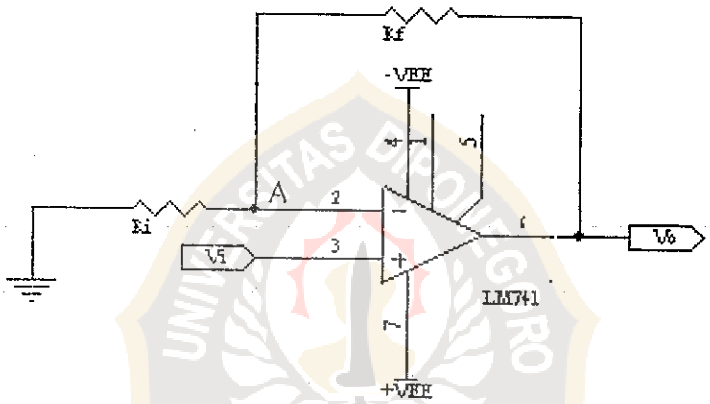
$$V_o = \frac{R_f}{Ri} V_i + V_i$$

$$V_o = \left(\frac{R_f}{Ri} + 1\right) V_i$$

sehingga

$$A_{CL} = \frac{V_o}{V_i}$$

$$A_{CL} = \frac{R_f}{R_i} + 1 \qquad \text{(A.3)}$$



Gambar A.3 Penguat Non-Inverting

Dengan menerapkan teorema superposisi pada rangkaian differensial amplifier maka didapatkan persamaan sebagai berikut:

$$V_{O..} = \left(\frac{R_f}{R_1} + 1\right) V_2 - \frac{R_f}{R_1} V_1 \qquad \text{(A.4)}$$

dimana V_2 adalah inputan positip dan V_1 adalah inputan negatip penguat operasional. Persamaan diatas tidak seimbang karena pada inputan negatip dan inputan positip tidak memiliki penguatan yang sama. Hal ini dapat dilakukan dengan mengatur nilai tegangan yang masuk pada inputan positip, yaitu dengan

menambahkan rangkaian pembagi tegangan seperti pada rangkaian penguat instrumentasi bagian penguat differensial. Dalam kondisi seimbang akan didapatkan persamaan (Aston, 1990).

$$V_{out} = (R_f/R_1)(V_2-V_1) \qquad (A.5)$$

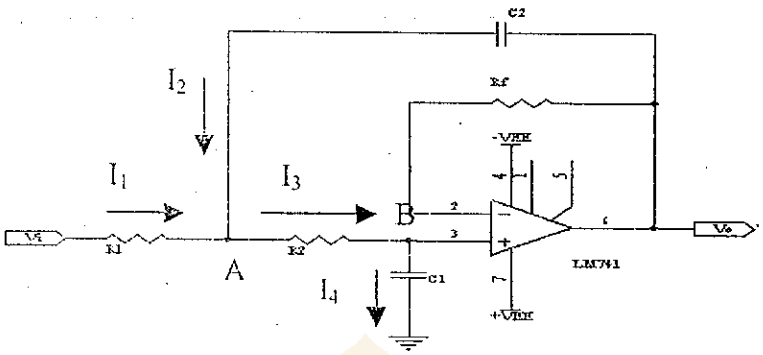
Sehingga penguatan total Instrumentasi Amplifier adalah (Aston, 1990):

$$A_V = A_{VBuffer} \cdot A_{VDifferensial}$$
$$A_V = \left(\frac{R_0 + R_1 + R_2}{R_0}\right)\left(\frac{R_f}{R_1}\right) \qquad (A.6)$$

LAMPIRAN B

LAMPIRAN B

Penurunan Persamaan Filter Lolos Rendah –40dB



Gambar B.1 Rangkaian Filter Lolos Rendah –40dB

Pada perancangan alat digunakan filter lolos rendah dengan penguatan –40dB. Ini berarti pada frekuensi *cut-off* setiap kenaikan 1 dekade terjadi pelemahan sebesar 40 kali. Berikut ini penurunan persamaan filter lolos bawah – 40dB (Aston, 1990).

$$I_1 = \frac{V_1 - V_A}{R_1} \tag{B.1}$$

$$I_2 = \frac{V_0 - V_A}{Xc_2} \tag{B.2}$$

$$I_3 = \frac{V_A - V_B}{R_2} \tag{B.3}$$

$$I_4 = \frac{V_B - 0}{Xc_1} \tag{B.4}$$

$E_d = 0$, sehingga $V_B = V_0$

$$I_3 = I_4$$

sehingga

$$\frac{V_A - V_0}{R_2} = \frac{V_0}{Xc_1}$$

$$V_A - V_0 = R_2 Xc_1 V_0$$

$$V_A = R_2 Xc_1 V_0 + V_0$$

$$V_A = jR_2 \omega C_1 V_0 + V_0 \qquad \text{(B.5)}$$

$$I_3 = I_1 + I_2$$

sehingga

$$\frac{V_A - V_0}{R_2} = \frac{V_1 - V_A}{R_1} + \frac{V_0 - V_A}{Xc_2}$$

$$\frac{V_A - V_0}{R_2} = \frac{V_1 - V_A}{R_1} + (V_0 - V_A) j\omega C_2$$

$$\frac{jR_2\omega C_1 V_0 + V_0 - V_0}{R_2} = \frac{V_1 - jR_2\omega C_1 V_0 - V_0}{R_1} + (V_0 - jR_2\omega C_1 V_0 - V_0) j\omega C_2$$

$$j\omega C_1 V_0 = \frac{V_1 - jR_2\omega C_1 V_0 - V_0}{R_1} + \omega^2 C_1 C_2 R_2 V_0$$

$$j\omega C_1 R_1 V_0 = V_1 - V_0 - j\omega C_1 R_2 V_0 + \omega^2 C_1 C_2 R_1 R_2 V_0$$

$$V_1 = V_0 + j\omega C_1 R_2 V_0 - \omega^2 C_1 C_2 R_1 R_2 V_0 + j\omega C_1 R_1 V_0$$

$$V_1 = V_0 \left(1 + j\omega C_1 R_2 - \omega^2 C_1 C_2 R_1 R_2 + j\omega C_1 R_1\right)$$

$$V_1 = V_0 \left(\left(1 - \omega^2 C_1 C_2 R_1 R_2\right) + j\left(\omega C_1 R_2 + \omega C_1 R_1\right)\right)$$

$$A_{CL} = \frac{V_0}{V_1} = \frac{1}{\left(1 - \omega^2 C_1 C_2 R_1 R_2\right) + j\left(\omega C_1 R_2 + \omega C_1 R_1\right)} \qquad \text{(B.6)}$$

Jika

$$R_1 = R_2 = R$$

$$C_2 = 2C_1$$

maka

$$A_{CL} = \frac{1}{\left(1 - 2\omega^2 C_1^{\,2} R^2\right) + j\left(\omega C_1 R_2 + \omega C_1 R\right)} \qquad \text{(B.7)}$$

Syarat terjadinya frekuensi *cutt off* adalah

$$\omega = \omega c \rightarrow A_{CL} = 0{,}707 \angle -90°$$

$$1 - 2\omega_C^2 C_1^2 R^2 = 0$$

$$\omega_C^2 = \frac{1}{2C_1^2 R^2}$$

$$\omega_C = \frac{0{,}707}{C_1 R} \qquad \text{(B.8)}$$

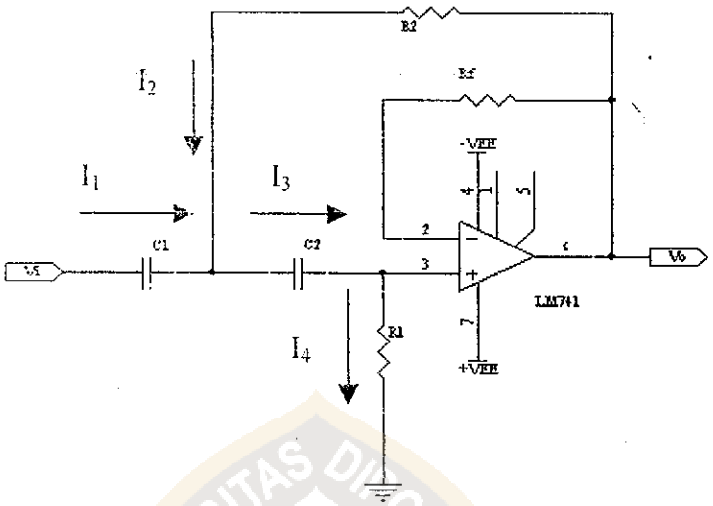
Berikut ini prosedur desain filter lolos bawah –40dB.

1. Dipilih harga ω_c atau f_c
2. Dipilih $R_1 = R_2 = R$ (10K – 100K)
3. Dicari harga C_1 dari persamaan $C_1 = 0{,}707/\omega_c R$
4. Dipilih $C_2 = 2C_1$
5. Dipilih harga $R_f = 2R$

LAMPIRAN C

LAMPIRAN C

Penurunan Persamaan Filter Lolos Tinggi 40dB



Gambar C.1 Rangkaian Filter
Lolos Tinggi +40dB

Pada perancangan alat digunakan filter lolos tinggi dengan penguatan +40dB. Ini berarti pada frekuensi *cut-off* setiap kenaikan 1 dekade terjadi penguatan sebesar 40 kali. Berikut ini penurunan persamaan filter lolos atas +40dB (Aston, 1990).

$$I_1 = \frac{V_1 - V_A}{Xc_1} \tag{C.1}$$

$$I_2 = \frac{V_0 - V_A}{R_2} \tag{C.2}$$

$$I_3 = \frac{V_A - V_B}{Xc_2} \tag{C.3}$$

$$I_4 = \frac{V_B - 0}{R_1} \tag{C.4}$$

$E_d = 0$ sehingga $V_B = V_0$

$$I_3 = I_4$$

sehingga

$$\frac{V_A - V_0}{Xc_2} = \frac{V_0}{R_1}$$

$$V_A - V_0 = \frac{Xc_2 V_0}{R_1}$$

$$V_A = \frac{Xc_2 V_0}{R_1} + V_0$$

$$V_A = \frac{V_0}{j\omega R_1 C_2} + V_0 \qquad \text{(C.5)}$$

$$I_3 = I_1 + I_2$$

sehingga

$$\frac{V_A - V_0}{Xc_2} = \frac{V_1 - V_A}{Xc_1} + \frac{V_0 - V_A}{R_2}$$

$$j\omega C_2 (V_A - V_0) = j\omega C_1 (V_1 - V_A) + \frac{V_0 - V_A}{R_2}$$

$$j\omega C_2 \left(\frac{V_0}{j\omega R_1 C_2} + V_0 - V_0 \right) = j\omega C_1 \left(V_1 - \frac{V_0}{j\omega R_1 C_2} - V_0 \right) + \frac{V_0 - \frac{V_0}{j\omega R_1 C_2} - V_0}{R_2}$$

$$\frac{j\omega C_2 V_0}{j\omega R_1 C_2} = j\omega C_1 \left(V_1 - \frac{V_0}{j\omega R_1 C_2} - V_0 \right) - \frac{V_0}{j\omega R_1 R_2 C_2}$$

$$\frac{C_2 V_0}{R_1 C_2} = j\omega C_1 V_1 - \frac{C_1 V_0}{R_1 C_2} - j\omega C_1 V_0 - \frac{V_0}{j\omega R_1 R_2 C_2}$$

$$\frac{C_2 V_0}{R_1 C_2} + \frac{C_1 V_0}{R_1 C_2} + j\omega C_1 V_0 + \frac{V_0}{j R_1 R_2 \omega C_2} = j\omega C_1 V_1$$

$$\left(\frac{C_2}{R_1 C_2} + \frac{C_1}{R_1 C_2} + j\omega C_1 + \frac{1}{j R_1 R_2 \omega C_2} \right) V_0 = j\omega C_1 V_1$$

$$\left(\frac{C_1 + C_2}{R_1 C_2} + j\omega C_1 + \frac{1}{j\omega R_1 R_2 C_2} \right) V_0 = j\omega C_1 V_1$$

$$\left(\frac{C_1 + C_2}{j\omega R_1 C_1 C_2} + 1 - \frac{1}{\omega^2 R_1 R_2 C_1 C_2} \right) V_0 = V_1$$

$$\left(1-\frac{1}{\omega^2 R_1 R_2 C_1 C_2}-j\frac{C_1+C_2}{\omega R_1 C_1 C_2}\right)V_0 = V_1$$

$$\left(1-\frac{1}{\omega^2 R_1 R_2 C_1 C_2}-j\frac{1}{\omega R_1}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)\right)V_0 = V_1$$

$$A_{CL} = \frac{V_0}{V_1} = \frac{1}{\left(1-\frac{1}{\omega^2 R_1 R_2 C_1 C_2}-j\frac{1}{\omega R_1}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)\right)} \qquad \text{(C.6)}$$

Jika

$C_1 = C_2 = C$

$R_1 = 2R_2$

maka

$$A_{CL} = \frac{1}{\left(1-\frac{1}{\omega^2 2R_2^2 C^2}-j\frac{2}{\omega 2R_2 C}\right)} \qquad \text{(C.7)}$$

Syarat terjadinya frekuensi *cutt off* adalah

$\omega = \omega c \rightarrow A_{CL} = 0{,}707\angle 90°$

$$1-\frac{1}{\omega_C^2 2R_2^2 C^2} = 0$$

$$\omega_C^2 = \frac{1}{2R_2^2 C^2}$$

$$\omega_C = \frac{0{,}707}{R_2 C} \qquad \text{(C.8)}$$

Berikut ini prosedur desain filter lolos tinggi +40dB.

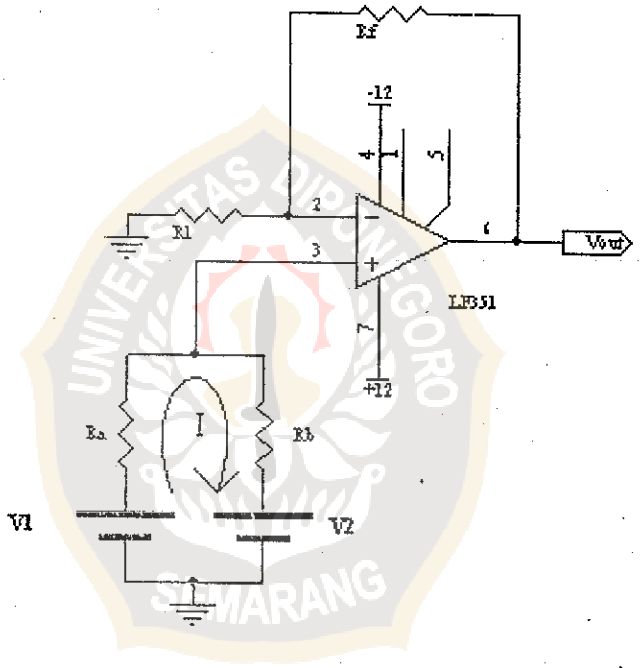
1. Dipilih harga ω_c atau f_c
2. Dipilih $C_1 = C_2 = C$ (0,001uF-0,1uF)
3. Dicari harga R dari persamaan $R_2 = 0{,}707/\omega_c C$
4. Dipilih $R_1 = 2R_2$
5. Dipilih harga $R_f = R_1$

LAMPIRAN D

LAMPIRAN D

Pembuktian Persamaan Penguat Penjumlah

Gambar D.1. adalah prinsip rangkaian penguat penjumlah yang dirancang untuk menggeser gelombang EKG kearah positip dengan memberikan nilai tegangan *DC*.



Gambar D.1 Rangkaian Penguat Penjumlah

Rangkaian ini pada dasarnya adalah rangkaian yang digunakan untuk menjumlahkan beberapa buah sinyal input (AC maupun DC) dengan perbesaran yang independen untuk masing-masing sinyal input tergantung kepada besarnya R_f dan besarnya R_I masing-masing input. Berikut ini penurunan persamaannya (Boylestad, 1992).

$$V_0 = \left(\frac{R_f}{R_1} + 1 \right) V_i \qquad \text{(D.1)}$$

karena

$$I = \frac{V_1 - V_2}{R_a + R_b} \qquad \text{(D.2)}$$

maka

$$V_i = R_b \left(\frac{V_1 - V_2}{R_a + R_b} \right) + V_2$$

$$V_i = \frac{R_b}{R_a + R_b} V_1 - \frac{R_b}{R_a + R_b} V_2 + V_2$$

$$V_i = \frac{R_b}{R_a + R_b} V_1 + \frac{R_a}{R_a + R_b} V_2$$

sehingga

$$V_0 = \left(\frac{R_f}{R_1} + 1 \right) \left(\frac{R_b}{R_a + R_b} V_1 + \frac{R_a}{R_a + R_b} V_2 \right) \qquad \text{(D.3)}$$

jika

$$R_a = R_b = R_1 = R$$

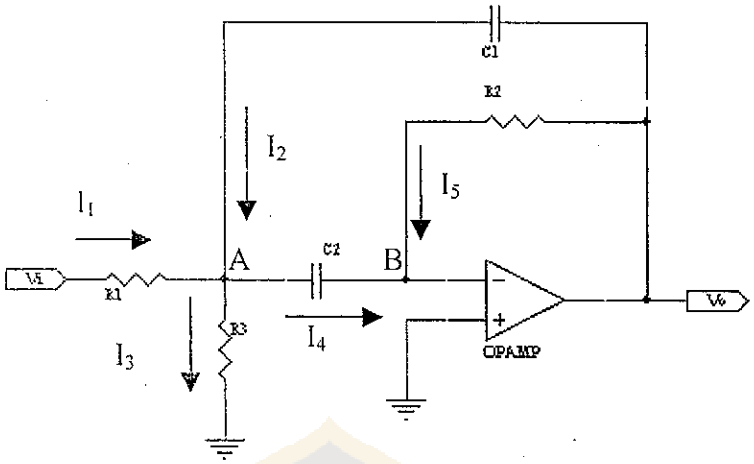
maka

$$V_0 = V_1 + V_2 \qquad \text{(D.4)}$$

LAMPIRAN E

LAMPIRAN E

Pembuktian Persamaan Band Pass Filter



Gambar E.1 Rangkaian Band Pass Filter

$$I_1 = \frac{V_1 - V_A}{R_1} \quad \text{(E.1)}$$

$$I_2 = \frac{V_0 - V_A}{Xc_1} \quad \text{(E.2)}$$

$$I_3 = \frac{V_A - 0}{R_3} \quad \text{(E.3)}$$

$$I_4 = \frac{V_A - V_B}{Xc_2} \quad \text{(E.4)}$$

$$I_5 = \frac{V_0 - V_B}{R_2} \quad \text{(E.5)}$$

V_B adalah virtual ground sehingga $V_B = 0$.

Pada titik B berlaku persamaan:

$$I_2 = -I_5$$
$$\frac{V_A}{Xc_2} = -\frac{V_0}{R_2}$$
$$V_A = -\frac{V_0 Xc_2}{R_2} \qquad \text{(E.6)}$$

Pada titik A berlaku persamaan:

$$I_1 + I_2 = I_3 + I_4$$
$$\frac{V_1 - V_A}{R_1} + \frac{V_0 - V_A}{Xc_1} = \frac{V_A}{R_3} + \frac{V_A}{Xc_2}$$
$$\frac{V_1}{R_1} - \frac{V_A}{R_1} + \frac{V_0}{Xc_1} - \frac{V_A}{Xc_1} = \frac{V_A}{R_3} + \frac{V_A}{Xc_2}$$
$$\frac{V_1}{R_1} = \frac{V_A}{R_1} - \frac{V_0}{Xc_1} + \frac{V_A}{Xc_1} + \frac{V_A}{R_3} + \frac{V_A}{Xc_2}$$
$$\frac{V_1}{R_1} = V_A\left(\frac{1}{R_1} + \frac{1}{Xc_1} + \frac{1}{R_3} + \frac{1}{Xc_2}\right) - \frac{V_0}{Xc_1}$$
$$\frac{V_1}{R_1} = \left(-\frac{V_0 Xc_2}{R_2}\right)\left(\frac{1}{R_1} + \frac{1}{Xc_1} + \frac{1}{R_3} + \frac{1}{Xc_2}\right) - \frac{V_0}{Xc_1}$$
$$\frac{V_1}{R_1} = (-V_0)\left(\frac{Xc_2}{R_1 R_2} + \frac{Xc_2}{R_2 Xc_1} + \frac{Xc_2}{R_2 R_3} + \frac{Xc_2}{R_2 Xc_2} + \frac{R_2 Xc_2}{R_2 Xc_2 Xc_1}\right)$$
$$\frac{V_1}{R_1} = (-V_0)\left(\frac{\frac{1}{j\omega C_2}}{R_1 R_2} + \frac{\frac{1}{j\omega C_2}}{R_2 - \frac{1}{j\omega C_1}} + \frac{\frac{1}{j\omega C_2}}{R_2 R_3} + \frac{1}{R_2} + \frac{1}{\frac{1}{j\omega C_1}}\right)$$
$$\frac{V_1}{R_1} = (-V_0)\left(\frac{1}{j\omega C_2 R_1 R_2} + \frac{1}{R_2 j\omega C_2 \frac{1}{j\omega C_1}} + \frac{1}{j\omega C_2 R_2 R_3} + \frac{1}{R_2} + j\omega C_1\right)$$

$$\frac{V_1}{R_1} = (-V_0)\left(\frac{1}{j\omega C_2 R_1 R_2} + \frac{C_1}{R_2 C_2} + \frac{1}{j\omega C_2 R_2 R_3} + \frac{1}{R_2} + j\omega C_1\right)$$

$$\frac{V_1}{R_1} = (-V_0)\left(\frac{-j}{\omega C_2 R_1 R_2} + \frac{C_1}{R_2 C_2} + \frac{-j}{\omega C_2 R_2 R_3} + \frac{1}{R_2} + j\omega C_1\right)$$

$$\frac{V_1}{R_1} = (-V_0)\left(\left(\frac{1}{R_2} + \frac{C_1}{R_2 C_2}\right) + j\left(\omega C_1 - \frac{1}{\omega C_2 R_1 R_2} - \frac{1}{\omega C_2 R_2 R_3}\right)\right)$$

$$\frac{V_0}{V_1} = (-)\frac{\frac{1}{R_1}}{\left(\frac{1}{R_2} + \frac{C_1}{R_2 C_2}\right) + j\left(\omega C_1 - \frac{1}{\omega C_2 R_1 R_2} - \frac{1}{\omega C_2 R_2 R_3}\right)}$$

Jika

$C_1 = C_2 = C$

maka

$$A_{CL} = \frac{V_0}{V_1} = (-)\frac{\frac{1}{R_1}}{\left(\frac{1}{R_2} + \frac{C}{R_2 C}\right) + j\left(\omega C - \frac{1}{\omega C R_1 R_2} - \frac{1}{\omega C R_2 R_3}\right)}$$

$$A_{CL} = (-)\frac{\frac{1}{R_1}}{\left(\frac{2}{R_2}\right) + j\left(\omega C - \frac{1}{\omega C R_1 R_2} - \frac{1}{\omega C R_2 R_3}\right)} \qquad \text{(E.7)}$$

Dari gambar E.2. dapat dilihat bahwa supaya A_{CL}=A_r maka bagian imaginer harus sama dengan nol, sehingga:

$$A_{CL} = A_r = (-)\frac{\frac{1}{R_1}}{\frac{2}{R_2}}$$

$$A_r = (-)\frac{R_2}{2R_1}$$

$$|A_r| = \frac{R_2}{2R_1} \qquad \text{(E.8)}$$

Pada saat $\omega = \omega_L = \omega_H$, maka

$$|A_{CL}| = 0{,}707|A_r|$$

sehingga

$$0{,}707|A_r| = \frac{\frac{1}{R_1}}{\sqrt{\left(-\frac{2}{R_2}\right)^2 + \left(-\omega C + \frac{1}{\omega C R_1 R_2} + \frac{1}{\omega C R_2 R_3}\right)^2}}$$

$$\left(0{,}707|A_r| = \frac{\frac{1}{R_1}}{\sqrt{\left(-\frac{2}{R_2}\right)^2 + \left(-\omega C + \frac{1}{\omega C R_1 R_2} + \frac{1}{\omega C R_2 R_3}\right)^2}}\right)^2$$

karena

$$0{,}707 = \frac{1}{\sqrt{2}}$$

$$|A_r| = \frac{R_2}{2R_1}$$

maka

$$\left(\frac{1}{\sqrt{2}}\frac{R_2}{2R_1}\right)^2 = \left(\frac{\frac{1}{R_1}}{\sqrt{\left(-\frac{2}{R_2}\right)^2 + \left(-\omega C + \frac{1}{\omega C R_1 R_2} + \frac{1}{\omega C R_2 R_3}\right)^2}}\right)^2$$

$$\frac{1}{2}\frac{R_2^2}{4R_1^2} = \frac{\frac{1}{R_1^2}}{\left(-\frac{2}{R_2}\right)^2 + \left(-\omega C + \frac{1}{\omega C R_1 R_2} + \frac{1}{\omega C R_2 R_3}\right)^2}$$

$$\frac{1}{8}R_2^2 = \frac{1}{\left(-\frac{2}{R_2}\right)^2 + \left(-\omega C + \frac{1}{\omega C R_1 R_2} + \frac{1}{\omega C R_2 R_3}\right)^2}$$

$$\left(-\frac{2}{R_2}\right)^2 + \left(-\omega C + \frac{1}{\omega C R_1 R_2} + \frac{1}{\omega C R_2 R_3}\right)^2 = \frac{8}{R_2^2}$$

$$\frac{4}{R_2^2} - \frac{8}{R_2^2} + \left(-\omega C + \frac{1}{\omega C R_1 R_2} + \frac{1}{\omega C R_2 R_3}\right)^2 = 0$$

$$\frac{4}{R_2^2}-\frac{8}{R_2^2}+\left(-\omega C+\frac{1}{\omega CR_1R_2}+\frac{1}{\omega CR_2R_3}\right)^2=0$$

$$\left(-\omega C+\frac{1}{\omega CR_1R_2}+\frac{1}{\omega CR_2R_3}\right)^2-\frac{4}{R_2^2}=0$$

$$\left(-\omega C+\frac{1}{\omega CR_1R_2}+\frac{1}{\omega CR_2R_3}\right)^2-\left(\frac{2}{R_2}\right)^2=0$$

$$\left(-\omega C+\frac{1}{\omega CR_1R_2}+\frac{1}{\omega CR_2R_3}+\frac{2}{R_2}\right)\left(-\omega C+\frac{1}{\omega CR_1R_2}+\frac{1}{\omega CR_2R_3}-\frac{2}{R_2}\right)=0$$

maka

ω_{1234}

adalah

$$\frac{1\pm\sqrt{\frac{R_1R_3+R_1R_2+R_3R_2}{R_1R_3}}}{CR_2}-\omega C+\frac{1}{\omega CR_1R_2}+\frac{1}{\omega CR_2R_3}+\frac{2}{R_2}=0\Big|\times\omega R_2$$

$$-\omega^2CR_2+\frac{1}{CR_1}+\frac{1}{CR_3}+2\omega=0$$

$$\omega^2CR_2-2\omega-\frac{R_1+R_3}{R_1R_3C}=0$$

$$\omega_{12}=\frac{2\pm\sqrt{4-4CR_2\left(-\frac{R_1+R_3}{R_1R_3C}\right)}}{2CR_2}$$

$$\omega_{12}=\frac{1\pm\sqrt{1+R_2\left(\frac{R_1+R_3}{R_1R_3}\right)}}{CR_2}$$

$$\omega_{12}=\frac{1\pm\sqrt{1+\frac{R_1R_2+R_3R_2}{R_1R_3}}}{CR_2}$$

$$\omega_{12}=\frac{1\pm\sqrt{\frac{R_1R_3+R_1R_2+R_3R_2}{R_1R_3}}}{CR_2}$$

$$\omega_1 = \omega_H = \frac{1+\sqrt{\frac{R_1R_3 + R_1R_2 + R_3R_2}{R_1R_3}}}{CR_2} \qquad \text{(E.9)}$$

ω_2 *diabaikan*

$$-\omega C + \frac{1}{\omega CR_1R_2} + \frac{1}{\omega CR_2R_3} - \frac{2}{R_2} = 0 \Big| \times \omega R_2$$

$$-\omega^2 CR_2 + \frac{1}{CR_1} + \frac{1}{CR_3} - 2\omega = 0$$

$$\omega^2 CR_2 + 2\omega - \frac{R_1 + R_3}{R_1R_3C} = 0$$

$$\omega_{34} = \frac{-2 \pm \sqrt{4 + 4CR_2\left(\frac{R_1 + R_3}{R_1R_3C}\right)}}{2CR_2}$$

$$\omega_{34} = \frac{-1 \pm \sqrt{1 + R_2\left(\frac{R_1 + R_3}{R_1R_3}\right)}}{CR_2}$$

$$\omega_{34} = \frac{-1 \pm \sqrt{1 + \frac{R_1R_2 + R_3R_2}{R_1R_3}}}{CR_2}$$

$$\omega_{34} = \frac{-1 \pm \sqrt{\frac{R_1R_3 + R_1R_2 + R_3R_2}{R_1R_3}}}{CR_2}$$

$$\omega_3 = \omega_L = \frac{-1+\sqrt{\frac{R_1R_3 + R_1R_2 + R_3R_2}{R_1R_3}}}{CR_2} \qquad \text{(E.10)}$$

ω_4 *diabaikan*

$Bandwidth(BW) = \omega_H - \omega_L$

$$BW = \frac{1+\sqrt{\frac{R_1R_3 + R_1R_2 + R_3R_2}{R_1R_3}}}{CR_2} - \frac{-1+\sqrt{\frac{R_1R_3 + R_1R_2 + R_3R_2}{R_1R_3}}}{CR_2}$$

$$BW = \frac{2}{CR_2} \qquad \text{(E.11)}$$

saat

$\omega = \omega_r$

maka

$|A_{CL}| = |A_r|$

$$\frac{R_2}{2R_1} = \frac{\frac{1}{R_1}}{\sqrt{\left(-\frac{2}{R_2}\right)^2 + \left(-\omega C + \frac{1}{\omega C R_1 R_2} + \frac{1}{\omega C R_2 R_3}\right)^2}} \quad \text{dikuadratkan}$$

$$\frac{R_2^2}{4} = \frac{1}{\left(-\frac{2}{R_2}\right)^2 + \left(-\omega C + \frac{1}{\omega C R_1 R_2} + \frac{1}{\omega C R_2 R_3}\right)^2}$$

$$\frac{R_2^2}{4} = \frac{1}{\frac{4}{R_2^2} + \left(-\omega C + \frac{1}{\omega C R_1 R_2} + \frac{1}{\omega C R_2 R_3}\right)^2}$$

$$\frac{R_2^2}{4} + \left(-\omega C + \frac{1}{\omega C R_1 R_2} + \frac{1}{\omega C R_2 R_3}\right)^2 = \frac{R_2^2}{4}$$

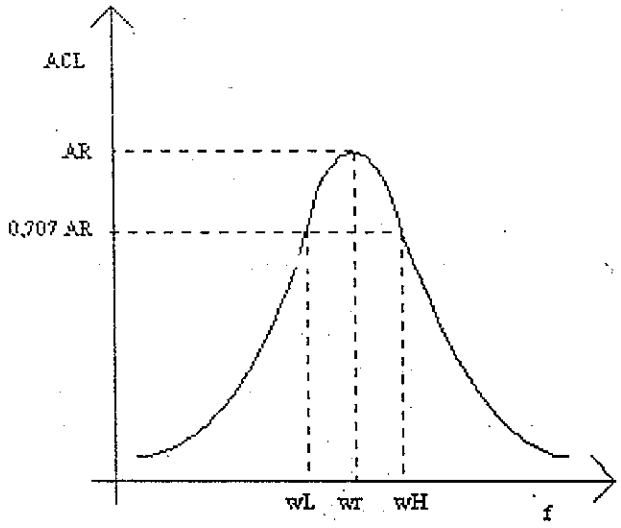
$$\left(-\omega C + \frac{1}{\omega C R_1 R_2} + \frac{1}{\omega C R_2 R_3}\right)^2 = 0$$

$$\left(\frac{-\omega^2 C^2 R_1 R_2 R_3 + R_1 + R_3}{\omega C R_1 R_2 R_3}\right)^2 = 0$$

$$-\omega^2 C^2 R_1 R_2 R_3 + R_1 + R_3 = 0$$

$$\omega^2 C^2 R_1 R_2 R_3 = R_1 + R_3$$

$$\omega = \frac{1}{C}\sqrt{\frac{R_1 + R_3}{R_1 R_2 R_3}} \qquad \text{(E.12)}$$



Gambar E.2 Respon Frekuensi Filter Band-Pass

Prosedur perencanaan Filter Band Pass adalah sebagai berikut:

1. Dipilih frekuensi tengah f_r , $|A_r|$ dan Bandwidth BW
2. Dipilih $C_1 = C_2$ diantara 0,001 – 0,1 uF
3. Dihitung R_2 dari persamaan:

$$R_2 = \frac{2}{B_w C}$$

4. Dihitung R_1 dari persamaan:

$$R_1 = \frac{R_2}{2|A_r|}$$

5. Dihitung R_3 dari persamaan

$$R_3 = \frac{R_2}{4Q^2 - 2|A_r|}$$

dengan

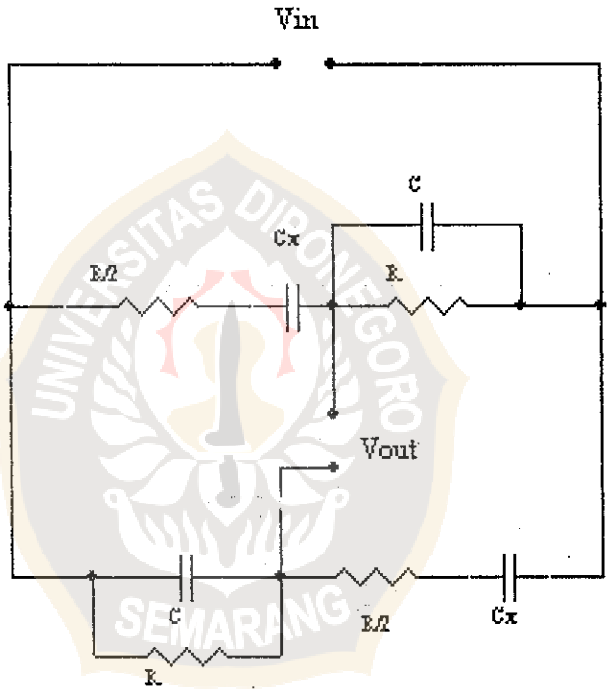
$$Q = \frac{\omega_r}{B_w}$$

LAMPIRAN F

LAMPIRAN F

Penurunan Persamaan Filter Band-Reject

Filter *band-reject* yang dirancang merupakan jenis filter *Twin T*, dengan konsep dasar jembatan setimbang impedansi seperti pada gambar F.1 (Williams, 1998). Adapun rangkaian filter *band-reject* pada gambar F.2



Gambar F.1 Ekuivalen Twin T

$$Z_1 = Z_4 = \frac{R}{2} + Xc_x \qquad \text{(F.1)}$$

$$Z_2 = Z_3 = \frac{RXc}{R + Xc} \qquad \text{(F.2)}$$

setimbang (F.3)

$$Z_1 Z_4 = Z_2 Z_3$$
$$Z_1^2 = Z_2^2$$
$$Z_1 = Z_2$$
$$C_x = 2C$$

$$\frac{R}{2} + \frac{1}{j2\omega C} = \frac{R\dfrac{1}{j\omega C}}{R + \dfrac{1}{j\omega C}}$$

$$\frac{j\omega RC + 1}{j\omega 2C} = \frac{\dfrac{R}{j\omega C}}{\dfrac{j\omega RC + 1}{j\omega C}}$$

$$\frac{j\omega RC + 1}{j\omega 2C} = \frac{R}{j\omega RC + 1}$$

$$(j\omega RC + 1)(j\omega RC + 1) = j2\omega RC$$

$$j^2\omega^2 R^2 C^2 + j2\omega RC + 1 = j2\omega RC$$

$$-\omega^2 R^2 C^2 + 1 = 0$$

$$\omega^2 R^2 C^2 = 1$$

$$\omega = \frac{1}{RC}$$

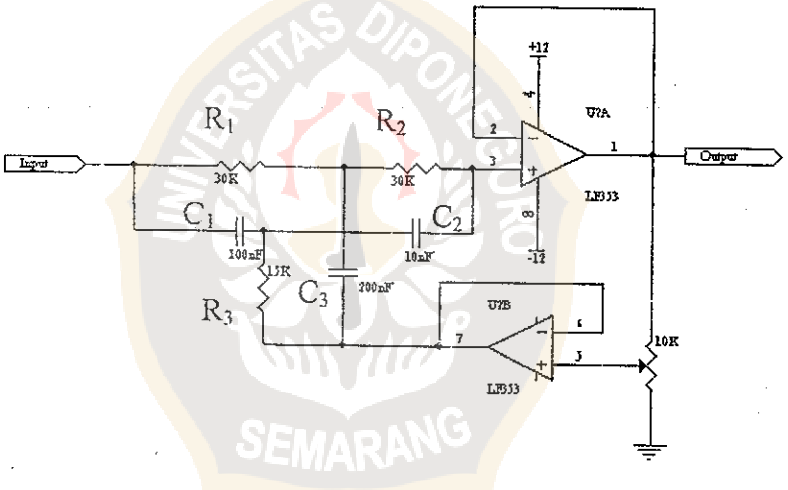
$$f = \frac{1}{2\pi RC} \qquad \text{(F.4)}$$

Prosedur perencanaan filter *band-reject* adalah sebagai berikut:

1. Tentukan f_c
2. Dipilih $R_1 = R_2 = R$ (10K – 100K)
3. Dipilih $R_3 = 0{,}5\ R$
4. Dihitung $C_1 = C_2 = C$ dari persamaan

$$C = \frac{1}{2\pi R f_0}$$

5. Dipilih $C_3 = 2C$



Gambar F.2 Rangkaian Filter Band-Reject

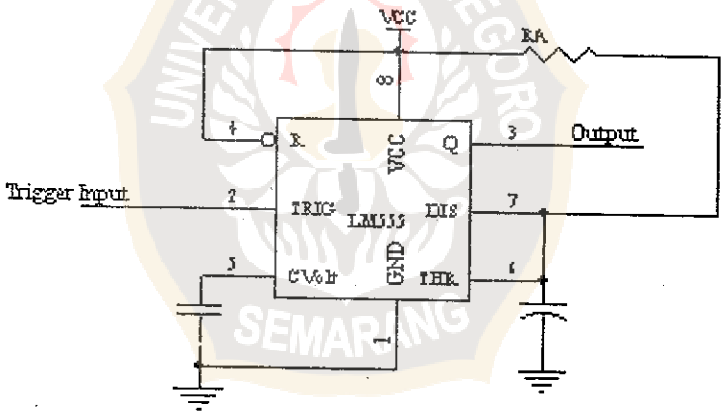
LAMPIRAN G

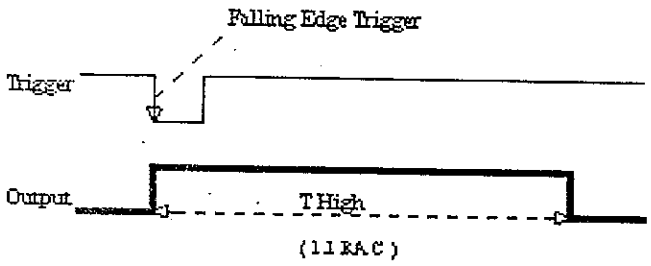
LAMPIRAN G

Pembuktian Persamaan Monostable Multivibrator

Rangkaian monostable multivibrator merupakan rangkaian yang akan memberikan sinyal output berupa kondisi High (tegangan positip dengan amplitudo tertentu sesuai dengan catu daya) jika diberi sinyal picu (Boylestad, 1992).

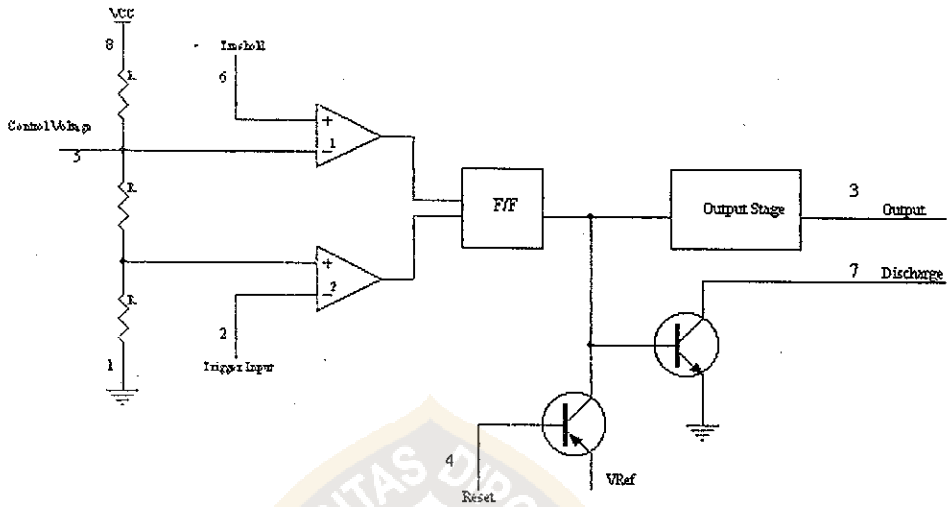
Pada rangkaian yang dirancang digunakan IC555 sebagai jantung rangkaian dengan catu daya 5 volt, dan memerlukan sinyal picu negatip. Gambar G.1 adalah rangkaian *monostable* yang dirancang.





Gambar G.1 Rangkaian Monostable Multivibrator

Gambar G.2 adalah skema IC 555 yang disederhanakan. Berikut ini penurunan persamaan *Monostable Multivibrator* dengan IC555 sebagai jantung rangkaian.



Gambar G.2. Skema IC555

V_C adalah tegangan pada kapasitor yang timbul akibat aktivitas penyimpanan muatan listrik. Muatan ini akan dibuang ketika sinyal picu diberikan pada pin 2 IC555. Bila sinyal picu telah berlalu, maka terjadi proses pengisian muatan ke kapasitor melalui tahanan R_A yang berlangsung sampai tegangan kapasitor (V_C) mencapai nilai $2V_{CC}/3$ ($t = t_C$, V_{CC} = supply tegangan).

$$V_C(t) = V_{CC} \cdot \left(1 - e^{-\frac{t}{\tau}}\right)$$

$$V_C(t) = V_{CC} - V_{CC} \cdot e^{-\frac{t}{\tau}}$$

saat

$$t = t_c \rightarrow V_C = \frac{2}{3} \cdot V_{CC}$$

$$\therefore \frac{2}{3} \cdot V_{CC} = V_{CC} - V_{CC} \cdot e^{-\frac{t_c}{\tau}}$$

$$-\frac{1}{3} \cdot V_{CC} = -V_{CC} \cdot e^{-\frac{t_c}{\tau}}$$

$$e^{-\frac{t_c}{\tau}} = \frac{1}{3}$$

$$\frac{t_c}{\tau} = \ln 3$$

$$t_c = \tau \cdot \ln 3$$

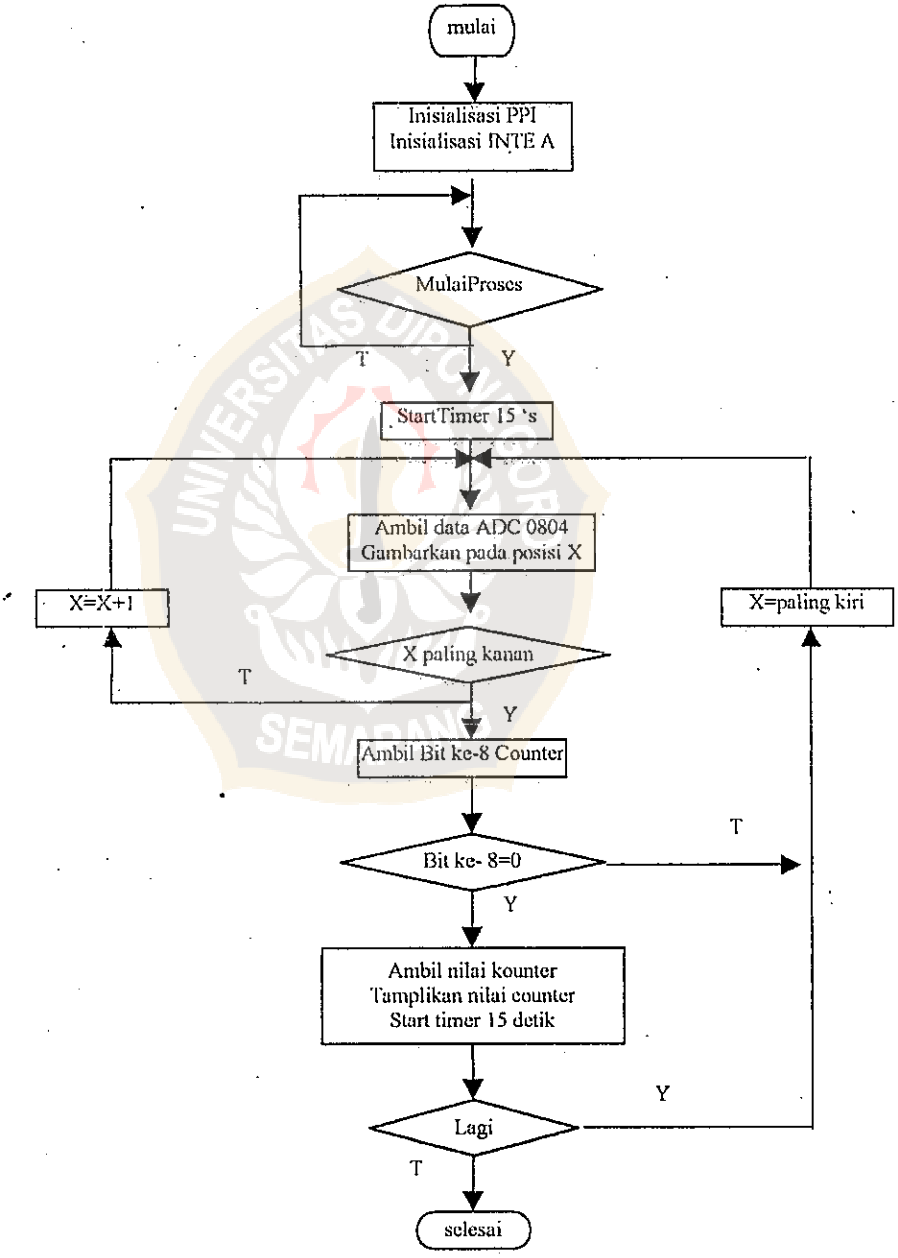
$$t_c = 1{,}1 \cdot RC \qquad \text{G.1}$$

LAMPIRAN H

LAMPIRAN H

DIAGRAM ALIR PROGRAM DAN LISTING PROGRAM

H.1. DIAGRAM ALIR PROGRAM



Gambar H.1 Diagram Alir Program

H.2. Listing Program

```
unit Revisi;

interface

uses
  Windows, Messages, SysUtils, Classes, Graphics, Controls, Forms, Dialogs,
  StdCtrls, ComCtrls, Buttons, ExtCtrls, Menus, HW_32;

Type
TForm1 = class(TForm)
    MainMenu1: TMainMenu;
    Keluar: TMenuItem;
    Help1: TMenuItem;
    VicHw321: TVicHw32;
    Image1: TImage;
    Bevel1: TBevel;
    BitBtn1: TBitBtn;
    Bevel3: TBevel;
    Bevel2: TBevel;
    Label1: TLabel;
    label2: TLabel;
    Bevel4: TBevel;
    StaticText1: TStaticText;
    StaticText2: TStaticTe; t;

    procedure FormCreate(Sender: TObject);
    procedure CanClose(Sender: TObject; Var CanClose: Boolean);
    procedure VicHw321Hwinterrupt(IrqNumber: Word);
    procedure BitBtn1Click(Sender: TObject);
    procedure Help1Click(Sender: TObject);
    procedure KeluarClick(Sender: TObject);
    procedure Button1Click(Sender: TObject);
    procedure Button2Click(Sender: TObject);

  private
    { Private declarations }
  public
    { Public declarations }

  end;

var
  Form1: TForm1;
  XTemp, YTemp,YValue, n, dataPic: Integer;
  DataInt: Byte;
  DataPixel: array[42..430,35..335] of integer;
  QRSCount: Byte;
  StatusCount: Byte;
  x: integer;

implementation

uses About, unit2;
```

```
{$R *.DFM}


{
Procedure yang digunakan untuk menghandle perintah Exit program.
Ditampilkan dialog Exit
}
procedure TForm1.CanClose(Sender: TObject; Var CanClose: Boolean);
begin
    // menampilkan dialog box
    if Application.MessageBox('Anda yakin ingin keluar dari program ini ?',
    'Confirmasi Exit',MB_YesNo or MB_IconQuestion or MB_DefButton1)= IDNo
    then CanClose := false
    else
    begin
        VicHW321.LPTIRQEnabled:= False;
    end;

    // proses menutup driver TVicHW321
    if CanClose then
    begin
        Form2.Visible:= False;
        VicHW321.CloseDriver;
    end;
end;

{
Procedure yang digunakan untuk meng-inizialisasi parameter2 yang dipakai dalam
program, termasuk didalamnya inisialisasi PPI 8255
}
procedure TForm1.FormCreate(Sender: TObject);
var
  IndX, IndY: Integer;
begin
    // proses menginstall driver TVicHW321
    VicHW321.OpenDriver('TVicDevice0');

    if not VicHW321.ActiveHW then
    begin
        ShowMessage('Driver GAGAL diinstall .. !');
    end;

    // proses inisialisasi LPT
    VicHW321.HardAccess:= True;
    VicHW321.LPTIRQEnabled:= False;
    VicHW321.LPTReadMode:= False;

    // Mengirimkan control word ke port Control PPI 8255
    with VicHW321 do
    begin
        Port[$378]:= $B2;       // sending  1011 0010
        Port[$37A]:= $00;       // address is pointed to port control PPI and WR is set to high
        Port[$37A]:= $04;       // set WR low and keep the adress, the formula is 0 or 4
        Port[$37A]:= $00;       // set WR high again and data should have reached control register
    end;

    // Aktivasi INT pada port A PPI dengan Enable INTE A
```

```
    with VicHW321 do
    begin
        Port[$378]:= $09;      // data will be sent  0000 1001
        Port[$37A]:= $00;      // address is pointed to port C PPI and WR is setted to high
        Port[$37A]:= $04;      // set WR low and keep the adress, the formula is 0 or 4
        Port[$37A]:= $00;      // set WR high again and data should have reached control register
    end;

    // Proses pengambilan dan penggambaran latar belakang
    // serta menunggu sampai proses penggambaran selesai dilakukan
    Image1.Picture.LoadFromFile('AQ.BMP');
    for x:=0 to 100 do Application.ProcessMessages;

    // proses pengambilan pixel demi pixel untuk proses penggambaran
    for IndX:= 42 to 430 do
       for IndY:= 35 to 335 do
          DataPixel[IndX,IndY]:= Canvas.Pixels[IndX ,IndY];

end;


// Proses yang ditangani selama Interupsi dengan IRQ 7
procedure TForm1.VicHw321HwInterrupt(IrqNumber: Word);
var
  IndY: integer;
begin
    // Menghindari terjadinya proses interupsi didalam interupsi yang bisa mengakibatkan
    // program menjadi liar

    VicHW321.LPTIRQEnabled:= False;

    // proses pengambilan nilai dari port A PPI
    with VicHW321 do
    begin
        Port[$37A]:= $03;      // point to address port A PPI and set RD high
        Port[$37A]:= $0B;      // set RD low and keep the adress point to port A PPI
        LPTReadMode:= True;
        dataInt:= port[$378];  // data is ready on port $378, and should have come into CPU Register
        Port[$37A]:= $03;      // set RD high, address unchanged
    end;


    // nilai nol grafik pada posisi 127
    dataPic:= (dataInt - 128)*2;


    // pengaturan skala pada grafik

    //11.811023622047244094488188976378 = 150/127

    // proses penghitungan posisi sebenarnya pada layar
    YValue:= 185 - round(1.171875 * DataPic);

    with Form1.Canvas do
    begin
       // bersihkan pixel pada posisi (n-1, nilai yang lalu )
```

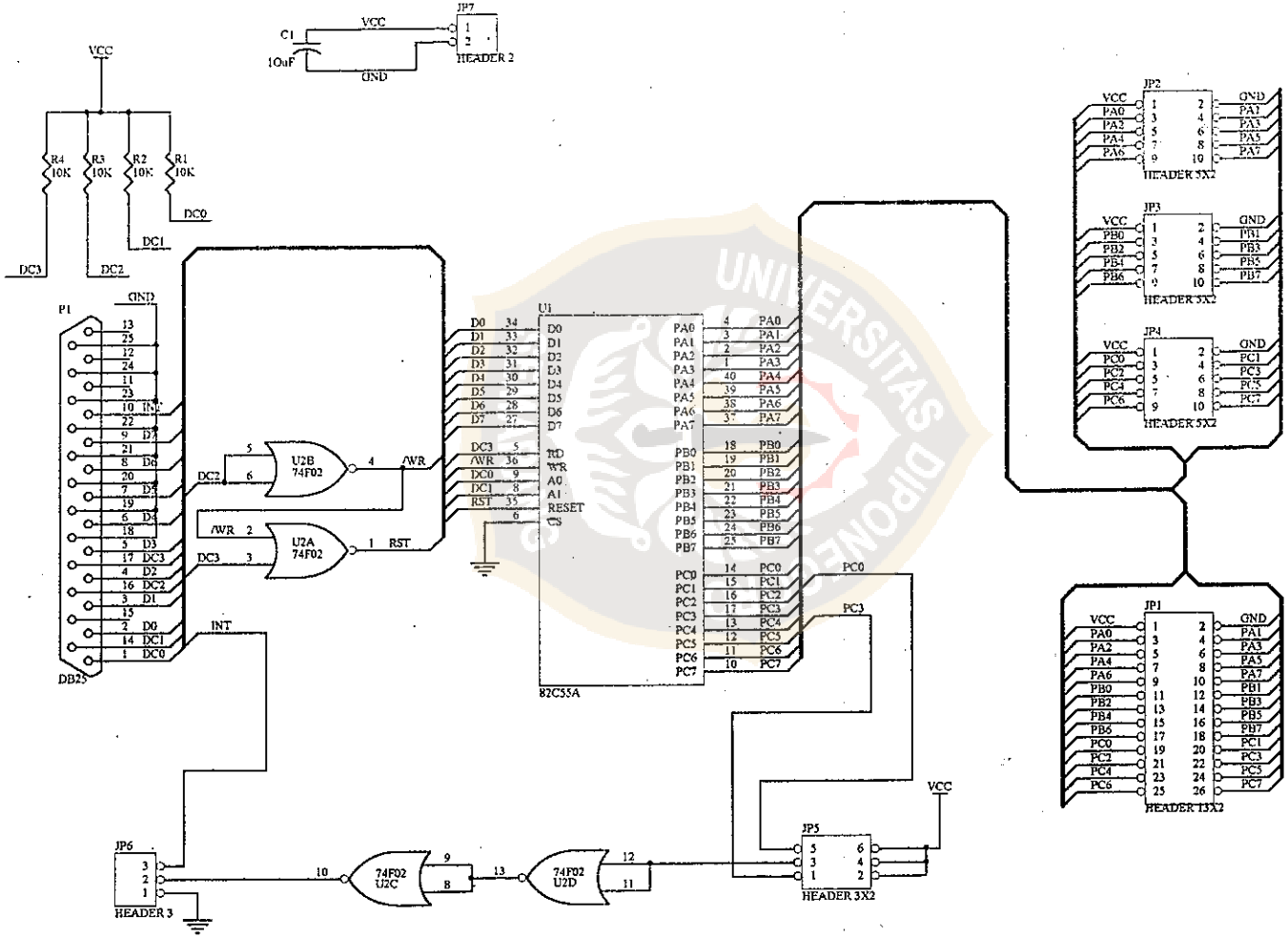
```
      for IndY := 35 to 335 do
      begin
         Pixels[n+1,IndY]:= DataPixel[n+1,IndY];
      end;

      // pindahkan pointer ke (n-1, nilai yang lalu)
      MoveTo(n,XTemp);
   end;

   // naikkan nilai n
   inc(n);

   // kembalikan n ke absis awal (42)
   if n >= 430 then
   begin

      // ==================================
      // proses pengambilan nilai counter

      with VicHW321 do
      begin
         Port[$37A] := $02;          // point to address port B PPI and set RD high
         Port[$37A] := $0A;          // set RD low and keep the adress point to port B PPI
         LPTReadMode:= True;         // LPT Read mode allowed
         StatusCount:= port[$378];   // data is ready on port $378, and should have come into CPU
Register
         Port[$37A] := $02;
      end;

      // proses pengambilan bit ke-0..6 pada data counter 7 bit
      QRSCount:= StatusCount;

      if (StatusCount and 128 = 0)then  // jika timer selesai menghitung, port B bit ke-7 = 0
      begin
         QRSCount:= QRSCount and 127;
         Label2.Caption:= IntToStr(QRSCount*4) + ' / menit';

         // proses pengiriman sinyal clear counter dan triger timer 15 second
         with VicHW321 do
         begin
            LPTReadMode:= False;

            Port[$378]:= $0F;      // data that will be sent  0000 1111
            Port[$37A]:= $00;      // address is pointed to port control PPI and WR is setted to high
            Port[$37A]:= $04;      // set WR low and keep the adress, the formula is 0 or 4
            Port[$37A]:= $00;      // set WR hihg again and data should have reached control register

            Port[$378]:= $0E;      // data that will be sent  0000 1110
            Port[$37A]:= $00;      // address is pointed to port control PPI and WR is setted to high
            Port[$37A]:= $04;      // set WR low and keep the adress, the formula is 0 or 4
            Port[$37A]:= $00;      // set WR hihg again and data should have reached control register

            Port[$378]:= $0F;      // data that will be sent  0000 1111
            Port[$37A]:= $00;      // address is pointed to port control PPI and WR is setted to high
            Port[$37A]:= $04;      // set WR low and keep the adress, the formula is 0 or 4
            Port[$37A]:= $00;      // set WR hihg again and data should have reached control register
         end;
```

```
        end;

        //=======================================

        // kembalikan absis pada posisi awal
        n:=41;
    end
    else
        if (YValue > 30) and (YValue < 335) then
        begin
            // proses penggambaran garis
            Form1.Canvas.LineTo(n,YValue);
            // nilai lalu = nilai sekarang
            XTemp:= YValue;
        end;

    // proses stop pada program
    if (BitBtn1.Caption= 'ST&OP') then VicHW321.LPTIRQEnabled:= True
    else VicHW321.LPTIRQEnabled:= False;
end;

// procedure yang digunakan untuk menghandle proses start dan stop
procedure TForm1.BitBtn1Click(Sender: TObject);
begin
    if (BitBtn1.Caption= 'ST&OP') then
    begin
        VicHW321.LPTIRQEnabled:= False;
        BitBtn1.Caption:='STA&RT';
        Help1.Enabled:= True;
        Keluar.Enabled:= True;
    end
    else
    begin

        // Siapkan setting counter dan timer
        with VicHW321 do
        begin
            LPTReadMode:= False;

            Port[$378]:= $0F;       // data that will be sent  0000 1110
            Port[$37A]:= $00;       // address is pointed to port control PPI and WR is setted to high
            Port[$37A]:= $04;       // set WR low and keep the adress, the formula is 0 or 4
            Port[$37A]:= $00;       // set WR hihg again and data should have reached control register

            Port[$378]:= $0E;       // data that will be sent  0000 1100
            Port[$37A]:= $00;       // address is pointed to port control PPI and WR is setted to high
            Port[$37A]:= $04;       // set WR low and keep the adress, the formula is 0 or 4
            Port[$37A]:= $00;       // set WR hihg again and data should have reached control register

            Port[$378]:= $0F;       // data that will be sent  0000 1110
            Port[$37A]:= $00;       // address is pointed to port control PPI and WR is setted to high
            Port[$37A]:= $04;       // set WR low and keep the adress, the formula is 0 or 4
            Port[$37A]:= $00;       // set WR hihg again and data should have reached control register
        end;

        // proses perubahan pada wajah program
        BitBtn1.Caption:= 'ST&OP';
```

```
        Help1.Enabled:= False;
        Keluar.Enabled:= False;

        if Form2.Visible= False then Form2.Visible:= True;
        Image1.Invalidate;     // canvas Activation
        n:=42;
        XTemp:= 185;
        VicHW321.LPTIRQEnabled:= True;
        VicHW321.UnmaskInterrupt(7);
    end;
end;


// procedure yang digunakan untuk menampilkan dialog about
procedure TForm1.Help1Click(Sender: TObject);
begin
    AboutBox.Timer1.Enabled:= True;
    AboutBox.Memo1.Top:= -8;
    if (AboutBox.Visible) then exit;    // to show the about box
    AboutBox.ShowModal;
end;

// procedure yang digunakan untuk merespon penekanan tombol exit
procedure TForm1.Keluar1Click(Sender: TObject);
begin
    Close;
end;

procedure TForm1.Button1Click(Sender: TObject);
begin
    with VicHW321 do
        begin
            LPTReadMode:= False;

            Port[$378]:= $0F;       // data that will be sent  0000 1110
            Port[$37A]:= $00;       // address is pointed to port control PPI and WR is setted to high
            Port[$37A]:= $04;       // set WR low and keep the adress, the formula is 0 or 4
            Port[$37A]:= $00;       // set WR hihg again and data should have reached control register

        end;
end;

procedure TForm1.Button2Click(Sender: TObject);
begin
    with VicHW321 do
        begin
            LPTReadMode:= False;

            Port[$378]:= $0F;       // data that will be sent  0000 1110
            Port[$37A]:= $00;       // address is pointed to port control PPI and WR is setted to high
            Port[$37A]:= $04;       // set WR low and keep the adress, the formula is 0 or 4
            Port[$37A]:= $00;       // set WR hihg again and data should have reached control register

        end;
end;

end.
```

```
unit About;

interface

uses Windows, SysUtils, Classes, Graphics, Forms, Controls, StdCtrls,
  Buttons, ExtCtrls;

type
  TAboutBox = class(TForm)
    Panel1: TPanel;
    ProgramIcon: TImage;
    ProductName: TLabel;
    Version: TLabel;
    Copyright: TLabel;
    Comments: TLabel;
    OKButton: TButton;
    Timer1: TTimer;
    Panel2: TPanel;
    Memo1: TMemo;
    Label1: TLabel;
    procedure OKButtonClick(Sender: TObject);
    procedure Timer1Timer(Sender: TObject);
  private
    { Private declarations }
  public
    { Public declarations }
  end;

var
  AboutBox: TAboutBox;


implementation

{$R *.DFM}

procedure TAboutBox.OKButtonClick(Sender: TObject);
begin
    Timer1.Enabled:= False;
    Close;
end;

procedure TAboutBox.Timer1Timer(Sender: TObject);
begin
    Timer1.Interval := 30;
    Memo1.Top := Memo1.Top - 1;
    if Memo1.Top = -890 then Memo1.Top := 0;
end;

end.
```

LAMPIRAN I



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Size: B	Number: 1		Revision: 0.01
Date: 20-Mar-2002		Sheet of 1 OF 1	
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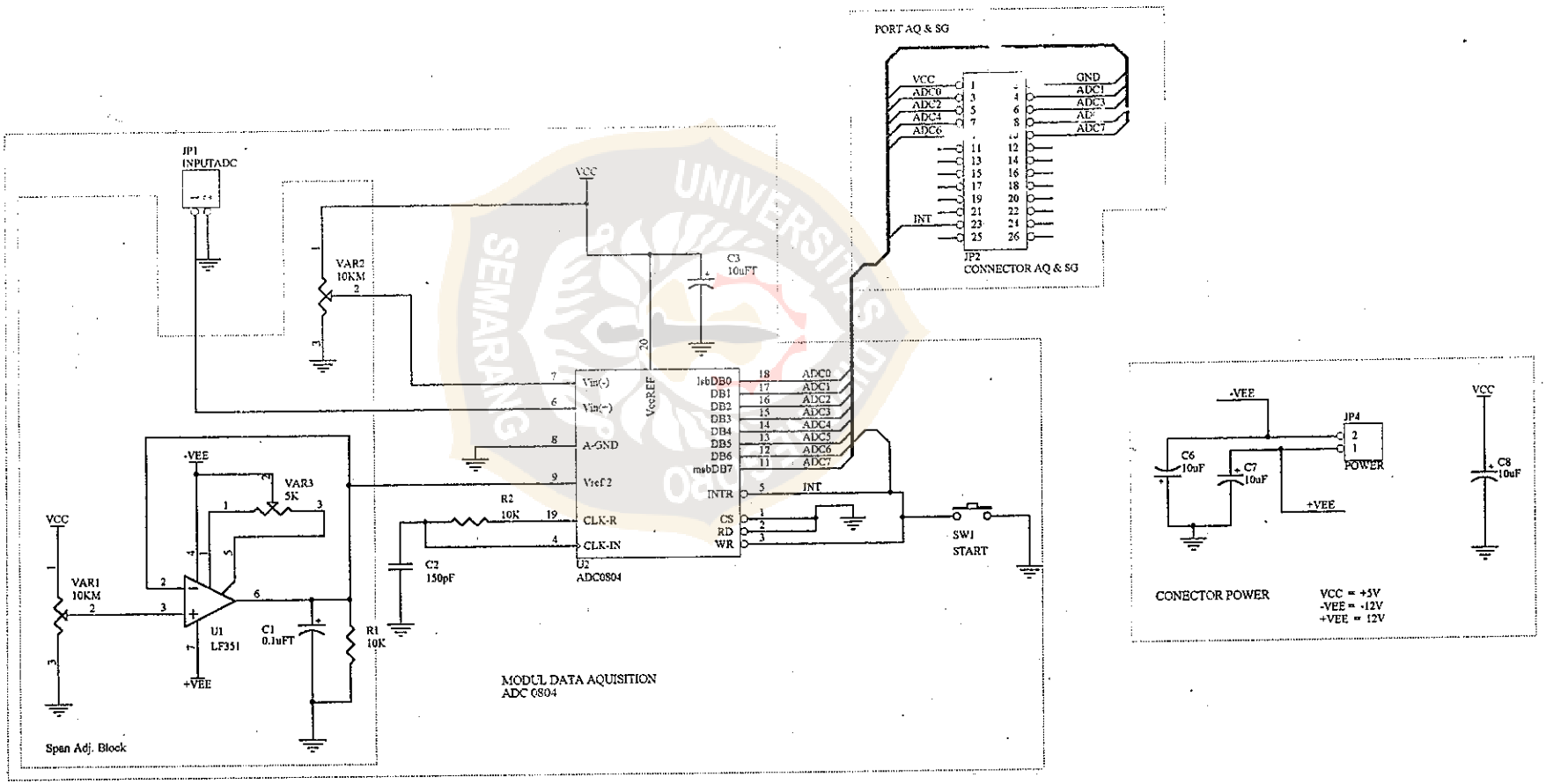

Title	Rangkaian Akuisisi ADC0804
Size	B
Number	1
Revision	0.1
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Sheet of	
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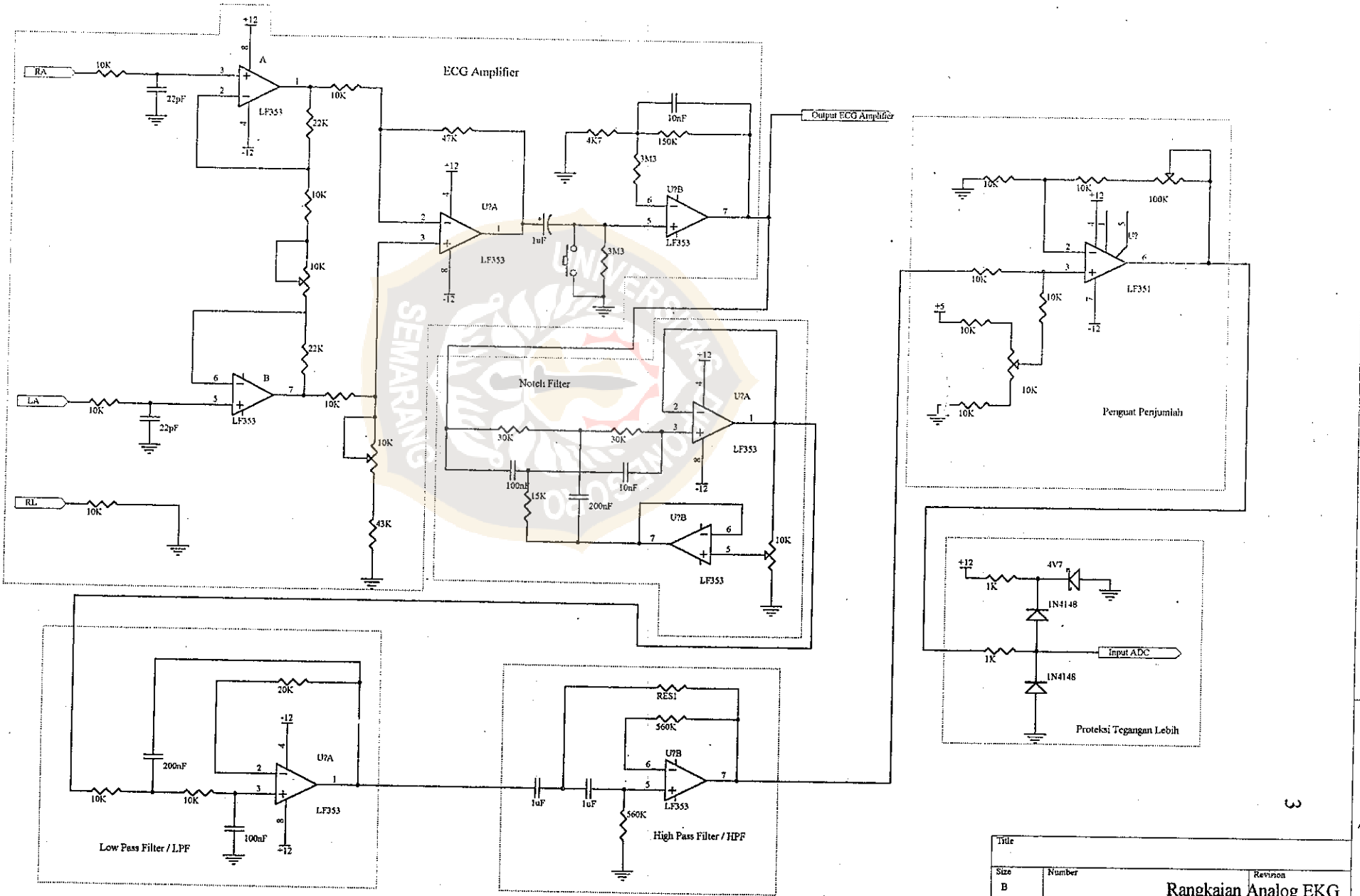
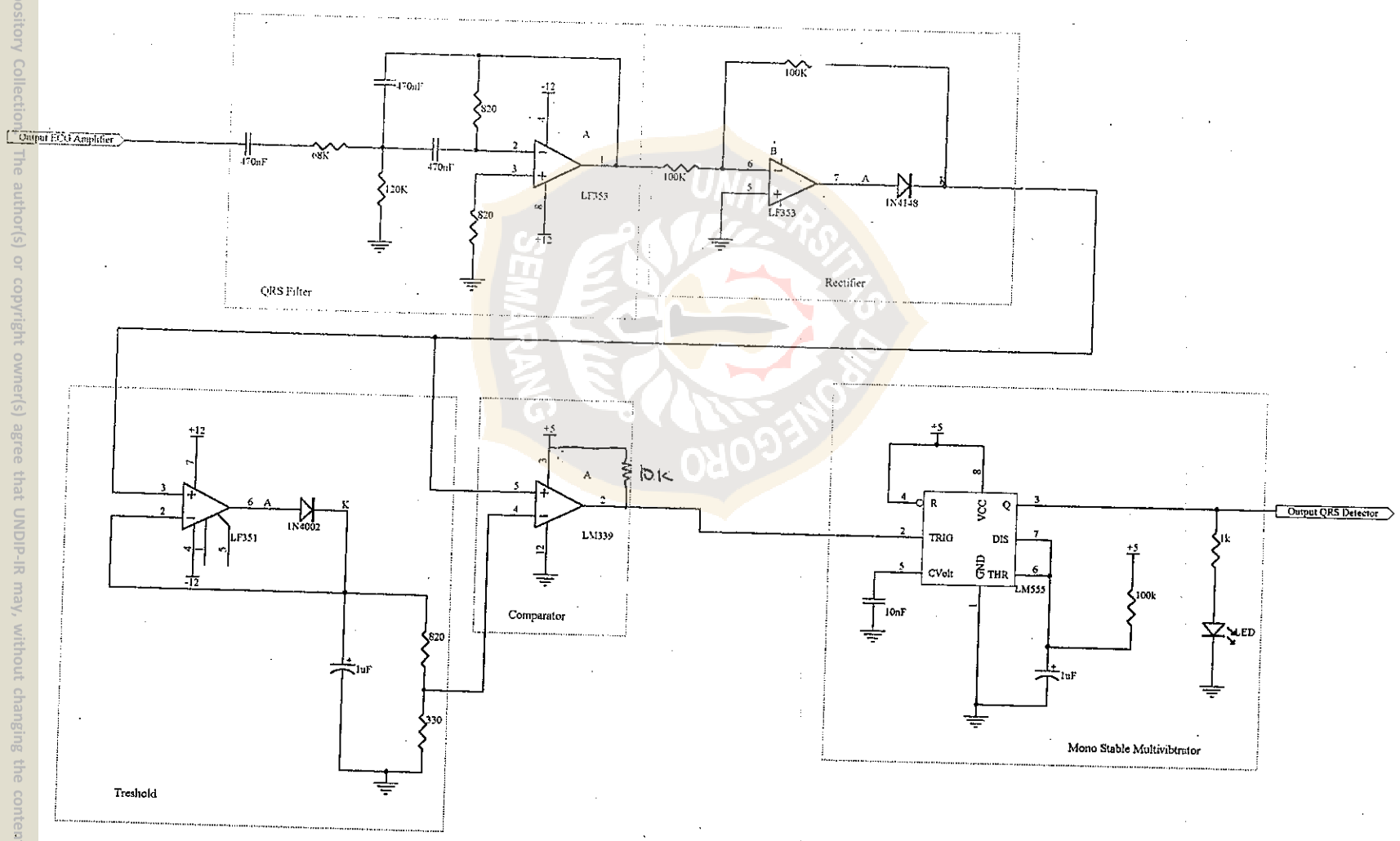
Drawn By:	XAS





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Size: B	Number	Revision
Date:	20-Mar-2002	Sheet of
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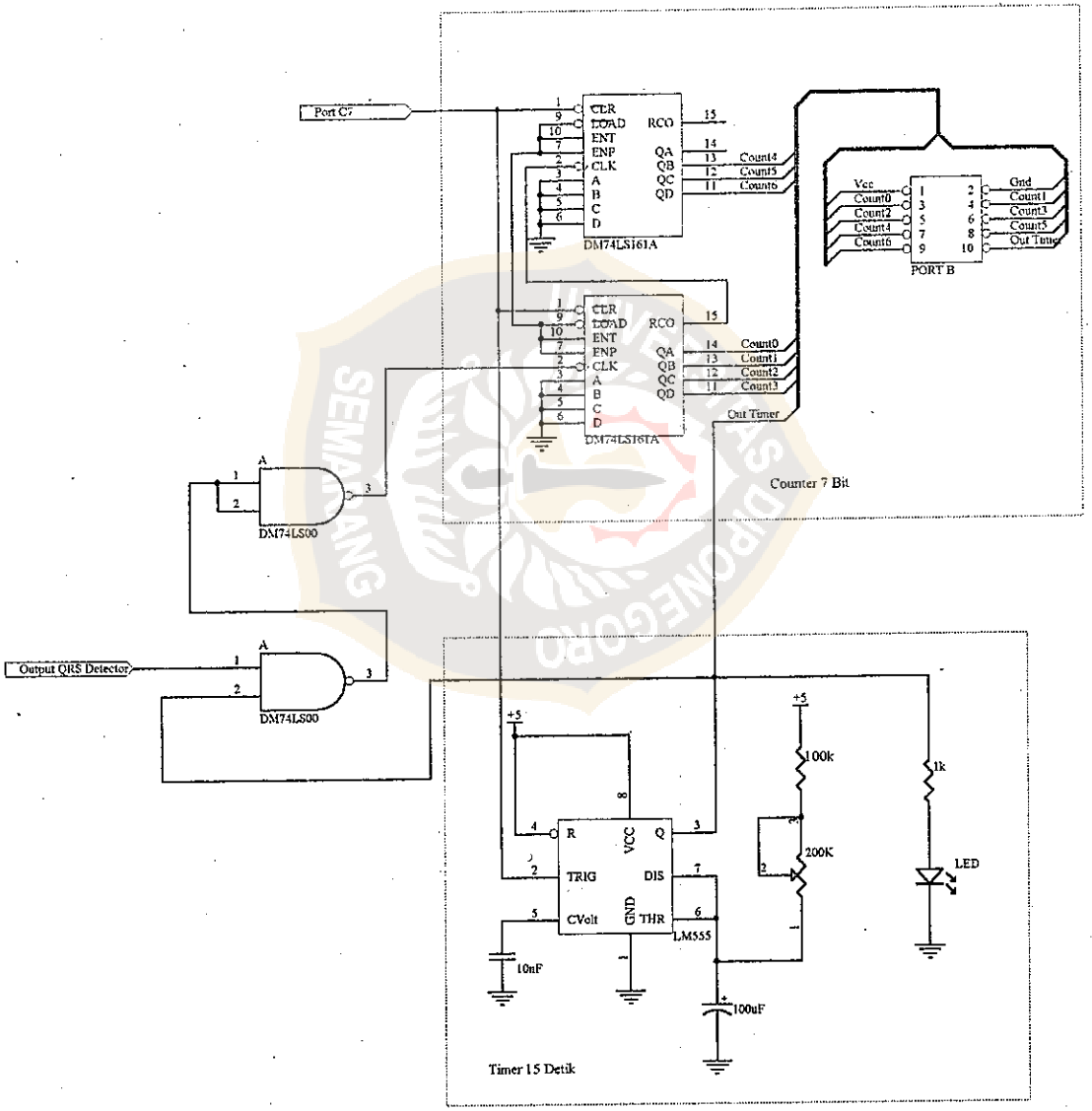


Title	Rangkaian Timer 15 Detik dan Counter 7 Bit		
Size B	Number		Revision
Date:	20-Mar-2002	Sheet of	
File:	C:\User\ADI\Circuitmaps\Aseg.DDB	Drawn By:	

LAMPIRAN J

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS00
Quad 2-Input NAND Gate

General Description

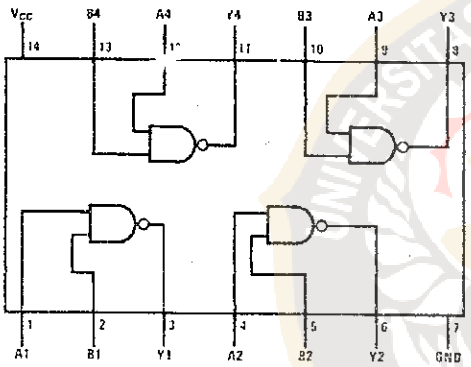
This device contains four independent gates each of which performs the logic NAND function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS00M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS00SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS00N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		0.8	1.6	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		2.4	4.4	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

FAIRCHILD SEMICONDUCTOR™

May 1986
Revised March 2000

DM74LS02
Quad 2-Input NOR Gate

General Description

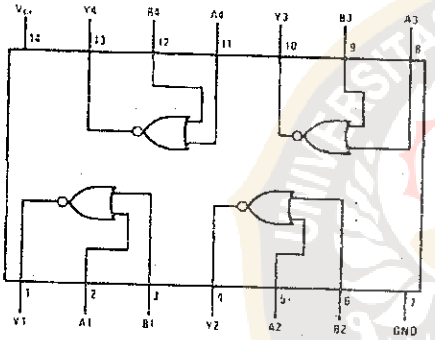
This device contains four independent gates each of which performs the logic NOR function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS02M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS02SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS02N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$Y = \overline{A + B}$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.40	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		1.6	3.2	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		2.8	5.4	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output		13		18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		10		15	ns

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

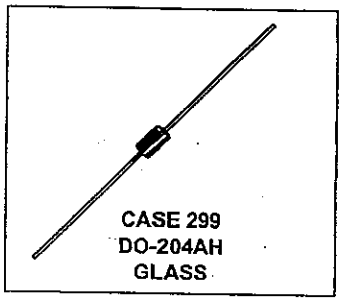
500 mW DO-35 Glass Zener Voltage Regulator Diodes

GENERAL DATA APPLICABLE TO ALL SERIES IN THIS GROUP

500 Milliwatt Hermetically Sealed Glass Silicon Zener Diodes

1N5985B SERIES
500 mW DO-35 GLASS

GLASS ZENER DIODES
500 MILLIWATTS
1.8–200 VOLTS



CASE 299
DO-204AH
GLASS

Specification Features:

- Complete Voltage Range — 1.8 to 200 Volts
- DO-204AH Package — Smaller than Conventional DO-204AA Package
- Double Slug Type Construction
- Metallurgically Bonded Construction

Mechanical Characteristics:

CASE: Double slug type, hermetically sealed glass
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 230°C, 1/16″ from case for 10 seconds
FINISH: All external surfaces are corrosion resistant with readily solderable leads
POLARITY: Cathode indicated by color band. When operated in zener mode, cathode will be positive with respect to anode
MOUNTING POSITION: Any
WAFER FAB LOCATION: Phoenix, Arizona
ASSEMBLY/TEST LOCATION: Seoul, Korea

MAXIMUM RATINGS (Motorola Devices)*

Rating	Symbol	Value	Unit
DC Power Dissipation and $T_L \leq 75°C$ Lead Length = 3/8″ Derate above T_L = 75°C	P_D	500 4	mW mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	– 65 to +200	°C

* Some part number series have lower JEDEC registered ratings.

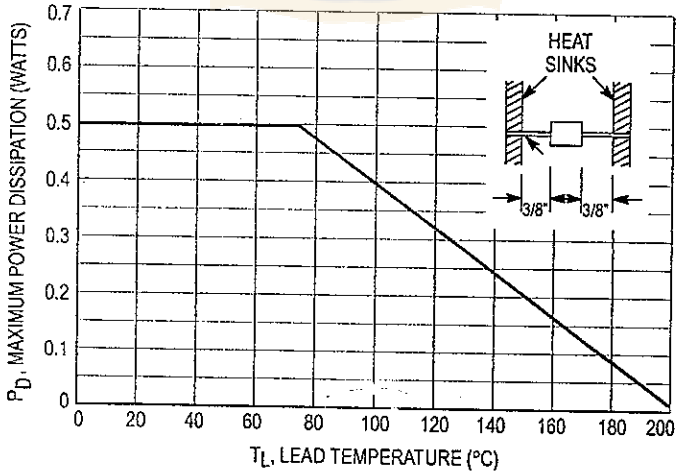


Figure 1. Steady State Power Derating

GENERAL DATA — 500 mW DO-35 GLASS

LECTRICAL CHARACTERISTICS (T_L = 30°C unless otherwise noted.) (V_F = 1.5 Volts Max @ I_F = 100 mAdc for all types.)

Motorola Type Number (Note 1)	Nominal Zener Voltage V_Z @ I_{ZT} Volts (Note 4)	Test Current I_{ZT} mA	Max Zener Impedance (Note 3)		Max Reverse Leakage Current		Max DC Zener Current I_{ZM} (Note 2)
			Z_{ZT} @ I_{ZT} Ohms	Z_{ZK} @ I_{ZK} = Ohms 0.25 mA	I_R µA	@ V_R Volts	
1N5985B	2.4	5	100	1800	100	1	208
1N5987B	3	5	95	2000	50	1	167
1N5988B	3.3	5	95	2200	25	1	152
1N5989B	3.6	5	90	2300	15	1	139
1N5990B	3.9	5	90	2400	10	1	128
1N5991B	4.3	5	88	2500	5	1	116
1N5992B	4.7	5	70	2200	3	1.5	106
1N5993B	***5.1***	***5***	***50***	***2050***	***2***	***2***	***98***
1N5994B	***5.6***	***5***	***25***	***1800***	***2***	***3***	***89***
1N5995B	6.2	5	10	1300	1	4	81
1N5996B	6.8	5	8	750	1	5.2	74
1N5997B	7.5	5	7	600	0.5	6	67
1N5998B	***8.2***	***5***	***7***	***600***	***0.5***	***6.5***	***61***
1N5999B	9.1	5	10	600	0.1	7	55
1N6000B	10	5	15	600	0.1	8	50
1N6002B	12	5	22	600	0.1	9.1	42
1N6003B	13	5	25	600	0.1	9.9	38
1N6004B	15	5	32	600	0.1	11	33
1N6006B	18	5	42	600	0.1	14	28

licates JEDEC Registered Data

TE 1. TOLERANCE AND VOLTAGE DESIGNATION

rance designation — Device tolerances of ±5% are indicated by a "B" suffix, ±2% by a suffix, ±1% by a "D" suffix.

TE 2.

s data was calculated using nominal voltages. The maximum current handling capability worst case basis is limited by the actual zener voltage at the operating point and the pow- lerating curve.

NOTE 3.

Z_{ZT} and Z_{ZK} are measured by dividing the ac voltage drop across the device by the ac current applied. The specified limits are for I_Z(ac) = 0.1 I_Z(dc) with the ac frequency = 1.0 kHz.

NOTE 4.

Nominal Zener Voltage (V_Z) is measured with the device junction in thermal equilibrium at the lead temperature of 30°C ±1°C and 3/8" lead length.

National Semiconductor

August 2000

LM139/LM239/LM339/LM2901/LM3302
Low Power Low Offset Voltage Quad Comparators

General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic— where the low power drain of the LM339 is a distinct advantage over standard comparators.

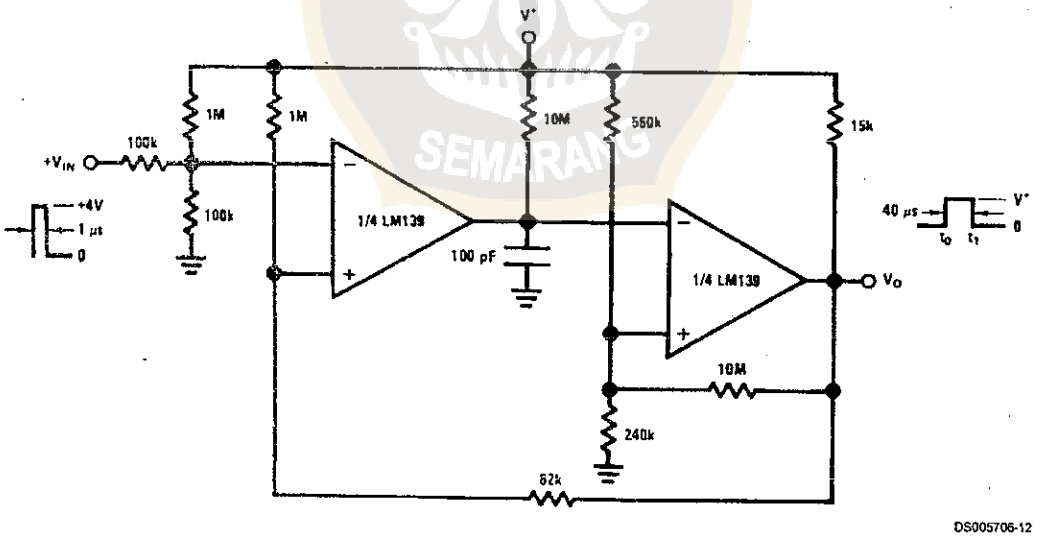
Features

- Wide supply voltage range
- LM139/139A Series 2 to 36 V_{DC} or ±1 to ±18 V_{DC}
- LM2901: 2 to 36 V_{DC} or ±1 to ±18 V_{DC}
- LM3302: 2 to 28 V_{DC} or ±1 to ±14 V_{DC}
- Very low supply current drain (0.8 mA) — independent of supply voltage
- Low input biasing current: 25 nA
- Low input offset current: ±5 nA
- Offset voltage: ±3 mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage: 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

One-Shot Multivibrator with Input Lock Out



DS005706-12

Absolute Maximum Ratings (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}	28 V_{DC} or ±14 V_{DC}
Differential Input Voltage (Note 8)	36 V_{DC}	28 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}	−0.3 V_{DC} to +28 V_{DC}
Input Current (V_{IN}<−0.3 V_{DC}), (Note 3)	50 mA	50 mA
Power Dissipation (Note 1)		
Molded DIP	1050 mW	1050 mW
Cavity DIP	1190 mW	
Small Outline Package	760 mW	
Output Short-Circuit to GND, (Note 2)	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
Operating Temperature Range		−40°C to +85°C
LM339/LM339A	0°C to +70°C	
LM239/LM239A	−25°C to +85°C	
LM2901	−40°C to +85°C	
LM139/LM139A	−55°C to +125°C	
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating (1.5 kΩ in series with 100 pF)	600V	600V

Electrical Characteristics

(V^+=5 V_{DC}, T_A = 25°C, unless otherwise stated)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)		1.0	2.0		1.0	2.0		2.0	5.0	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, (Note 5), V_{CM}=0V		25	100		25	250		25	100	nA_{DC}
Input Offset Current	$I_{IN(+)}$−$I_{IN(-)}$, V_{CM}=0V		3.0	25		5.0	50		3.0	25	nA_{DC}
Input Common-Mode Voltage Range	V^+=30 V_{DC} (LM3302, V^+=28 V_{DC}) (Note 6)	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V_{DC}
Supply Current	R_L=∞ on all Comparators,		0.8	2.0		0.8	2.0		0.8	2.0	mA_{DC}
	R_L=∞, V^+=36V,					1.0	2.5		1.0	2.5	mA_{DC}
	(LM3302, V^+=28 V_{DC}) .										
Voltage Gain	R_L≥15 kΩ, V^+=15 V_{DC} V_o= 1 V_{DC} to 11 V_{DC}	50	200		50	200		50	200		V/mV
Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}= 1.4 V_{DC}, V_{RL}=5 V_{DC}, R_L=5.1 kΩ		300			300			300		ns
Response Time	V_{RL}=5 V_{DC}, R_L=5.1 kΩ, (Note 7)		1.3			1.3			1.3		µs

lectrical Characteristics (Continued)

*=5 V_{DC}, T_A = 25°C, unless otherwise stated)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
put Sink Current	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0, V_O≤1.5 V_{DC}	6.0	16		6.0	16		6.0	16		mA_{DC}
uration Voltage	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0, I_{SINK}≤4 mA		250	400		250	400		250	400	mV_{DC}
put Leakage urrent	$V_{IN(+)}$=1 V_{DC}, $V_{IN(-)}$=0, V_O=5 V_{DC}		0.1			0.1			0.1		nA_{DC}

lectrical Characteristics

*=5 V_{DC}, T_A = 25°C, unless otherwise stated)

Parameter	Conditions	LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t Offset Voltage	(Note 9)		2.0	5.0		2.0	7.0		3	20	mV_{DC}
t Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, (Note 5), V_{CM}=0V		25	250		25	250		25	500	nA_{DC}
t Offset Current	$I_{IN(+)}$−$I_{IN(-)}$, V_{CM}=0V		5.0	50		5	50		3	100	nA_{DC}
t Common-Mode oltage Range	V+=30 V_{DC} (LM3302, V+=28 V_{DC}) (Note 6)	0		V+−1.5	0		V+−1.5	0		V+−1.5	V_{DC}
ply Current	R_L=∞ on all Comparators, R_L=∞, V+=36V, (LM3302, V+=28 V_{DC})		0.8 1.0	2.0 2.5		0.8 1.0	2.0 2.5		0.8 1.0	2.0 2.5	mA_{DC} mA_{DC}
tage Gain	R_L≥15 kΩ, V+=15 V_{DC} V_o= 1 V_{DC} to 11 V_{DC}	50	200		25	100		2	30		V/mV
ge Signal esponse Time	V_{IN}=TTL Logic Swing, V_{REF}= 1.4 V_{DC}, V_{RL}=5 V_{DC}, R_L=5.1 kΩ,		300			300			300		ns
sponse Time	V_{RL}=5 V_{DC}, R_L=5.1 kΩ, (Note 7)		1.3			1.3			1.3		µs
tput Sink Current	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0, V_O≤1.5 V_{DC}	6.0	16		6.0	16		6.0	16		mA_{DC}
uration Voltage	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0, I_{SINK}≤4 mA		250	400		250	400		250	500	mV_{DC}
tput Leakage Current	$V_{IN(+)}$=1 V_{DC}, $V_{IN(-)}$=0, V_O=5 V_{DC}		0.1			0.1			0.1		nA_{DC}

lectrical Characteristics

+ = 5.0 V_{DC}, (Note 4))

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ut Offset Voltage	(Note 9)			4.0			4.0			9.0	mV_{DC}
ut Offset Current	$I_{IN(+)}$−$I_{IN(-)}$, V_{CM}=0V			100			150			100	nA_{DC}
ut Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, V_{CM}=0V (Note 5)			300			400			300	nA_{DC}
ut Common-Mode ltage Range	V+=30 V_{DC} (LM3302, V+=28 V_{DC}) (Note 6)	0		V+−2.0	0		V+−2.0	0		V+−2.0	V_{DC}
turation Voltage	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0, I_{SINK}≤4 mA			700			700			700	mV_{DC}

Electrical Characteristics (Continued)

(V^+ = 5.0 V_{DC}, (Note 4))

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Leakage Current	$V_{IN(+)}$=1 V_{DC}, $V_{IN(-)}$=0, V_O=30 V_{DC}, (LM3302, V_O=28 V_{DC})			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s≥0 V_{DC} (or V⁻, if used), (Note 8)			36			36			36	V_{DC}

Electrical Characteristics

(V^+ = 5.0 V_{DC}, (Note 4))

Parameter	Conditions	LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			9.0		9	15			40	mV_{DC}
Input Offset Current	$I_{IN(+)}$−$I_{IN(-)}$, V_{CM}=0V			150		50	200			300	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, V_{CM}=0V (Note 5)			400		200	500			1000	nA_{DC}
Input Common-Mode Voltage Range	V^+=30 V_{DC} (LM3302, V^+=28 V_{DC}) (Note 6)			V^+−2.0	0		V^+−2.0	0		V^+−2.0	V_{DC}
Saturation Voltage	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0, I_{SINK}≤4 mA			700		400	700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)}$=1 V_{DC}, $V_{IN(-)}$=0, V_O=30 V_{DC}, (LM3302, V_O=28 V_{DC})			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s≥0 V_{DC} (or V⁻, if used), (Note 8)			36			36			28	V_{DC}

Note 1: For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 95°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small (P_D≤100 mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC} (at 25°)C.

Note 4: These specifications are limited to −55°C≤T_A≤+125°C, for the LM139/LM139A. With the LM239/LM239A, all temperature specifications are limited to −25°C≤T_A≤+85°C, the LM339/LM339A temperature specifications are limited to 0°C≤T_A≤+70°C, and the LM2901, LM3302 temperature range is −40°C≤T_A≤+85°C.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ −1.5V at 25°C, but either or both inputs can go to +30 V_{DC} without damage (25V for LM3302), independent of the magnitude of V^+.

Note 7: The response time specified is a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC}below the magnitude of the negative power supply, if used) (at 25°C).

Note 9: At output switch point, V_O=1.4 V_{DC}, R_S=0Ω with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to V^+ −1.5 V_{DC}), at 25°C. For LM3302, V^+ from 5 V_{DC} to 28 V_{DC}.

Note 10: Refer to RETS139AX for LM139A military specifications and to RETS139X for LM139 military specifications.

National Semiconductor

August 2000

LF353
Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

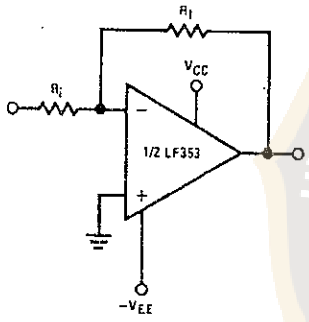
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Features

- Internally trimmed offset voltage: 10 mV
- Low input bias current: 50pA
- Low input noise voltage: 25 nV/√Hz
- Low input noise current: 0.01 pA/√Hz
- Wide gain bandwidth: 4 MHz
- High slew rate: 13 V/µs
- Low supply current: 3.6 mA
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion : ≤0.02%
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 µs

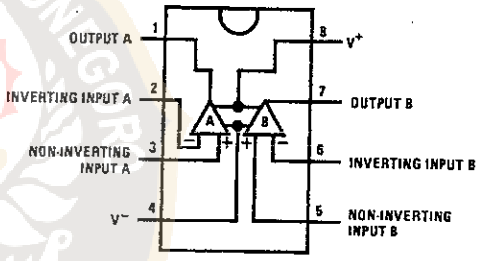
Typical Connection



DS005649-14

Connection Diagram

Dual-In-Line Package

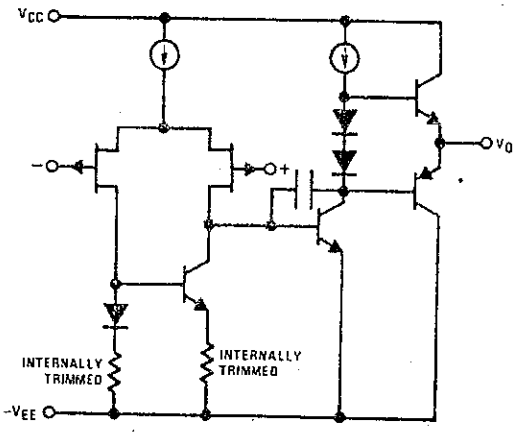


DS005649-17

Top View
Order Number LF353M, LF353MX or LF353N
See NS Package Number M08A or N08E

Simplified Schematic

1/2 Dual



DS005649-16

BI-FET II™ is a trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	(Note 2)
Operating Temperature Range	0°C to +70°C
T_j(MAX)	150°C
Differential Input Voltage	±30V
Input Voltage Range (Note 3)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 8)	1700V
θ_{JA} M Package	TBD

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

DC Electrical Characteristics

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10kΩ, T_A=25°C		5	10	mV
		Over Temperature			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ		10		µV/°C
I_{OS}	Input Offset Current	T_j=25°C, (Notes 5, 6)		25	100	pA
		T_j≤70°C			4	nA
I_B	Input Bias Current	T_j=25°C, (Notes 5, 6)		50	200	pA
		T_j≤70°C			8	nA
R_{IN}	Input Resistance	T_j=25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C	25	100		V/mV
		V_O=±10V, R_L=2 kΩ				
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage	V_S=±15V	±11	+15		V
	Range			−12		V
CMRR	Common-Mode Rejection Ratio	R_S≤ 10kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)	70	100		dB
I_S	Supply Current			3.6	6.5	mA

AC Electrical Characteristics

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A=25°C, f=1 Hz−20 kHz		−120		dB
		(Input Referred)				
SR	Slew Rate	V_S=±15V, T_A=25°C	8.0	13		V/µs
GBW	Gain Bandwidth Product	V_S=±15V, T_A=25°C	2.7	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25°C, R_S=100Ω,		16		nV/√Hz
		f=1000 Hz				
i_n	Equivalent Input Noise Current	T_j=25°C, f=1000 Hz		0.01		pA/√Hz

National Semiconductor

December 1995

LF351 Wide Bandwidth JFET Input Operational Amplifier

General Description

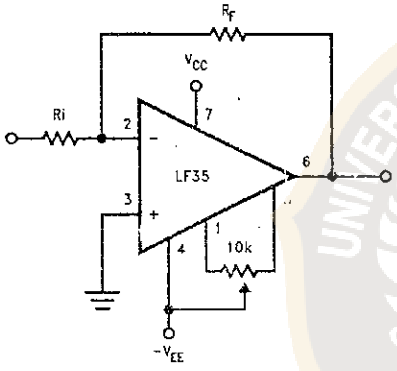
The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the LF351 is the better choice.

Features

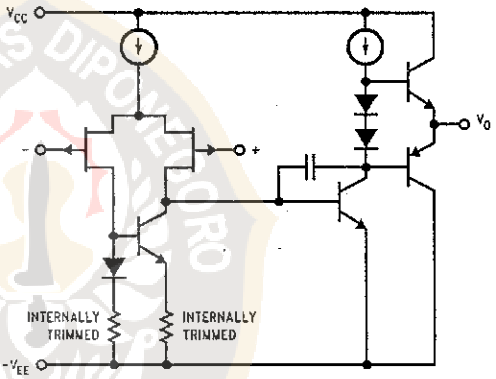
- Internally trimmed offset voltage — 10 mV
- Low input bias current — 50 pA
- Low input noise voltage — 25 nV/√Hz
- Low input noise current — 0.01 pA/√Hz
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/μs
- Low supply current — 1.8 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion $A_V=10$, $R_L=10k$, $V_O=20$ Vp-p, BW=20 Hz–20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

Typical Connection



TL/H/5648–11

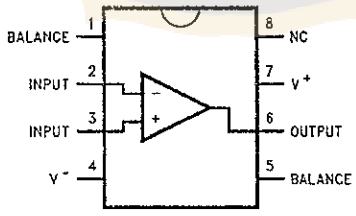
Simplified Schematic



TL/H/5648–12

Connection Diagrams

Dual-In-Line Package



TL/H/5648–13

Order Number LF351M or LF351N
See NS Package Number M08A or N08E

RRD-B30M125/Printed In U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Notes 1 and 6)	670 mW
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	
Metal Can	300°C
DIP	260°C

θ_{jA}	
N Package	120°C/W
M Package	TBD
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$ Over Temperature		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$		10		µV/°C
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 4) $T_j \leq 70°C$		25	100 4	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 4) $T_j \leq +70°C$		50	200 8	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2\ k\Omega$ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	70	100		dB
I_S	Supply Current			1.8	3.4	mA

AC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		13		V/μs
GBW	Gain Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, $f = 1000$ Hz		25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, $f = 1000$ Hz		0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on the thermal resistance, θ_{JA}.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

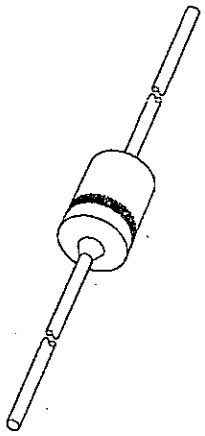
Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C \le T_A \le +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. From ±15V to ±5V.

Note 6: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

DATA SHEET



1N4148; 1N4446; 1N4448
High-speed diodes

Product specification
Supersedes data of April 1996
File under Discrete Semiconductors, SC01

1996 Sep 03

Philips Semiconductors

PHILIPS

High-speed diodes 1N4148; 1N4446; 1N4448

EATURES

Hermetically sealed leaded glass SOD27 (DO-35) package

High switching speed: max. 4 ns

General application

Continuous reverse voltage: max. 75 V

Repetitive peak reverse voltage: max. 75 V

Repetitive peak forward current: max. 450 mA.

PPLICATIONS

High-speed switching.

DESCRIPTION

The 1N4148, 1N4446, 1N4448 are high-speed switching diodes fabricated in planar technology, and encapsulated in hermetically sealed leaded glass SOD27 (DO-35) packages.

The diodes are type branded.

Fig.1 Simplified outline (SOD27; DO-35) and symbol.

MITING VALUES

accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage		–	75	V
V_R	continuous reverse voltage		–	75	V
I_F	continuous forward current	see Fig.2; note 1	–	200	mA
I_{FRM}	repetitive peak forward current		–	450	mA
I_{FSM}	non-repetitive peak forward current	square wave; T_j = 25 °C prior to surge; see Fig.4			
		t = 1 µs	–	4	A
		t = 1 ms	–	1	A
		t = 1 s	–	0.5	A
P_{tot}	total power dissipation	T_{amb} = 25 °C; note 1	–	500	mW
T_{stg}	storage temperature		–65	+200	°C
T_j	junction temperature		–	200	°C

ote

. Device mounted on an FR4 printed circuit-board; lead length 10 mm.

ELECTRICAL CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_F	forward voltage	see Fig.3			
	1N4148	I_F = 10 mA	–	1.0	V
	1N4446	I_F = 20 mA	–	1.0	V
	1N4448	I_F = 5 mA	0.62	0.72	V
		I_F = 100 mA	–	1.0	V
I_R	reverse current	V_R = 20 V; see Fig.5		25	nA
		V_R = 20 V; T_j = 150 °C; see Fig.5	–	50	µA
I_R	reverse current; 1N4448	V_R = 20 V; T_j = 100 °C; see Fig.5	–	3	µA
C_d	diode capacitance	f = 1 MHz; V_R = 0; see Fig.6		4	pF
t_{rr}	reverse recovery time	when switched from I_F = 10 mA to I_R = 60 mA; R_L = 100 Ω; measured at I_R = 1 mA; see Fig.7		4	ns
V_{fr}	forward recovery voltage	when switched from I_F = 50 mA; t_r = 20 ns; see Fig.8	–	2.5	V

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}tp}$	thermal resistance from junction to tie-point	lead length 10 mm	240	K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	lead length 10 mm; note 1	350	K/W

Note

1. Device mounted on a printed circuit-board without metallization pad.

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised April 2000

DM74LS161A • DM74LS163A
Synchronous 4-Bit Binary Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The DM74LS161A and DM74LS163A are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable input. The clear function for the DM74LS161A is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs LOW, regardless of the levels of clock, load, or enable inputs. The clear function for the DM74LS163A is synchronous; and a low level at the clear inputs sets all four of the flip-flop outputs LOW after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output.

Both count-enable inputs (P and T) must be HIGH to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. HIGH-to-LOW level transitions at the enable P or T inputs may occur, regardless of the logic level of the clock.

These counters feature a fully independent clock circuit. Changes made to control inputs (enable P or T or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

Features

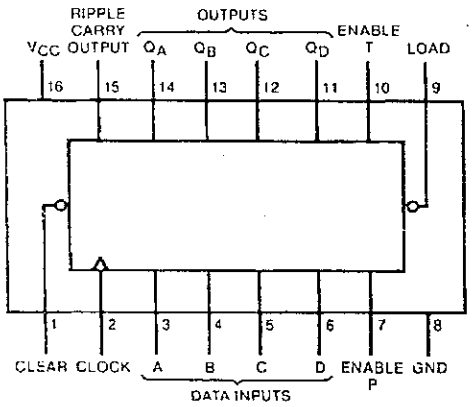
- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical propagation time, clock to Q output 14 ns
- Typical clock frequency 32 MHz
- Typical power dissipation 93 mW

Ordering Code:

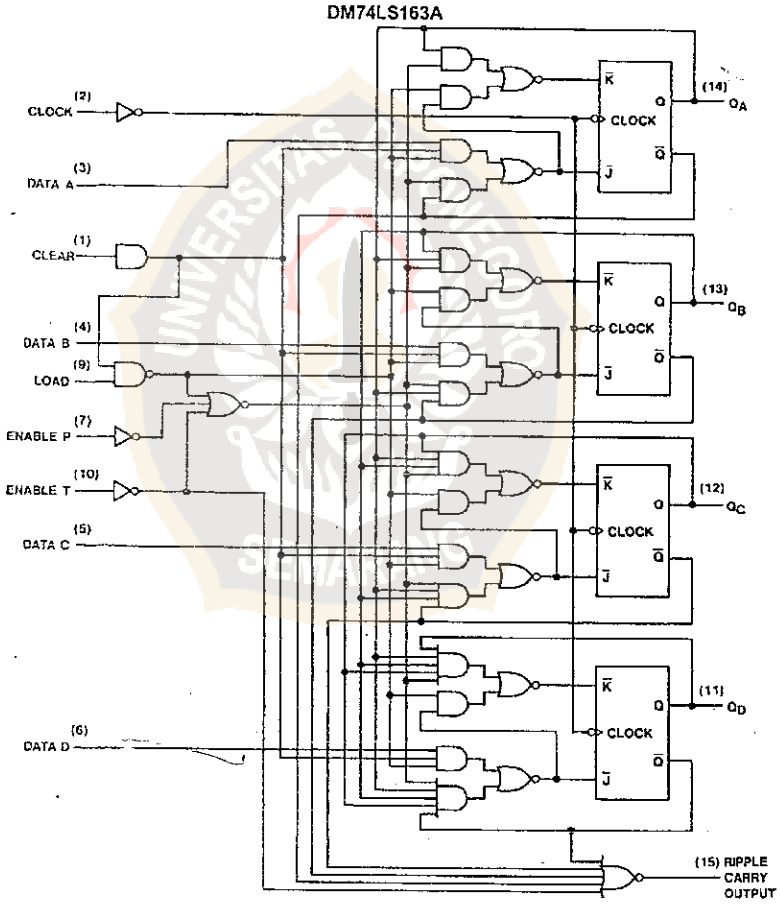
Order Number	Package Number	Package Description
DM74LS161AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS161AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74LS163AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS163AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



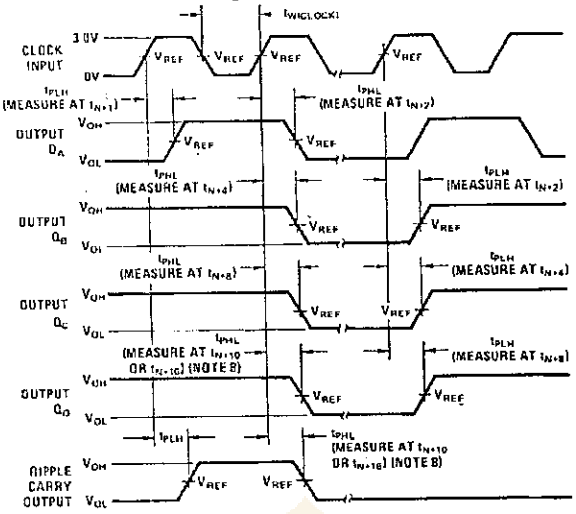
Logic Diagram



The DM74LS161A is similar, however, the clear buffer is connected directly to the flip-flops.

Parameter Measurement Information

Switching Time Waveforms



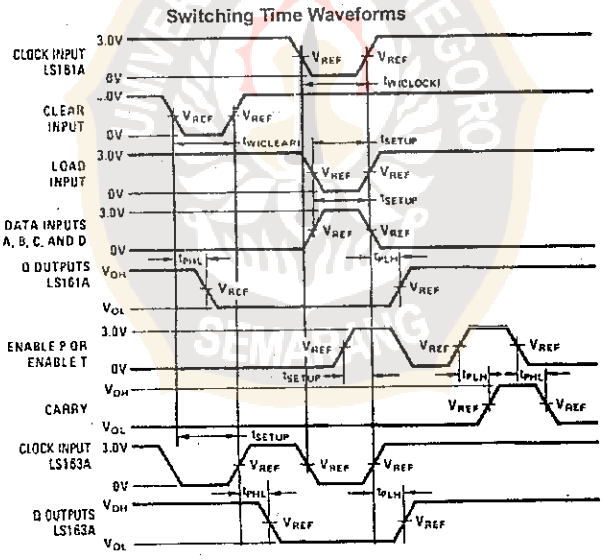
The input pulses are supplied by generators having the following characteristics:
PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_R \leq 10$ ns, $t_F \leq 10$ ns.

Vary PRR to measure f_{MAX}.

Outputs Q_D and carry are tested at t_{N+16} where t_N is the bit time when all outputs are LOW.

$V_{REF} = 1.5V$.

Switching Time Waveforms



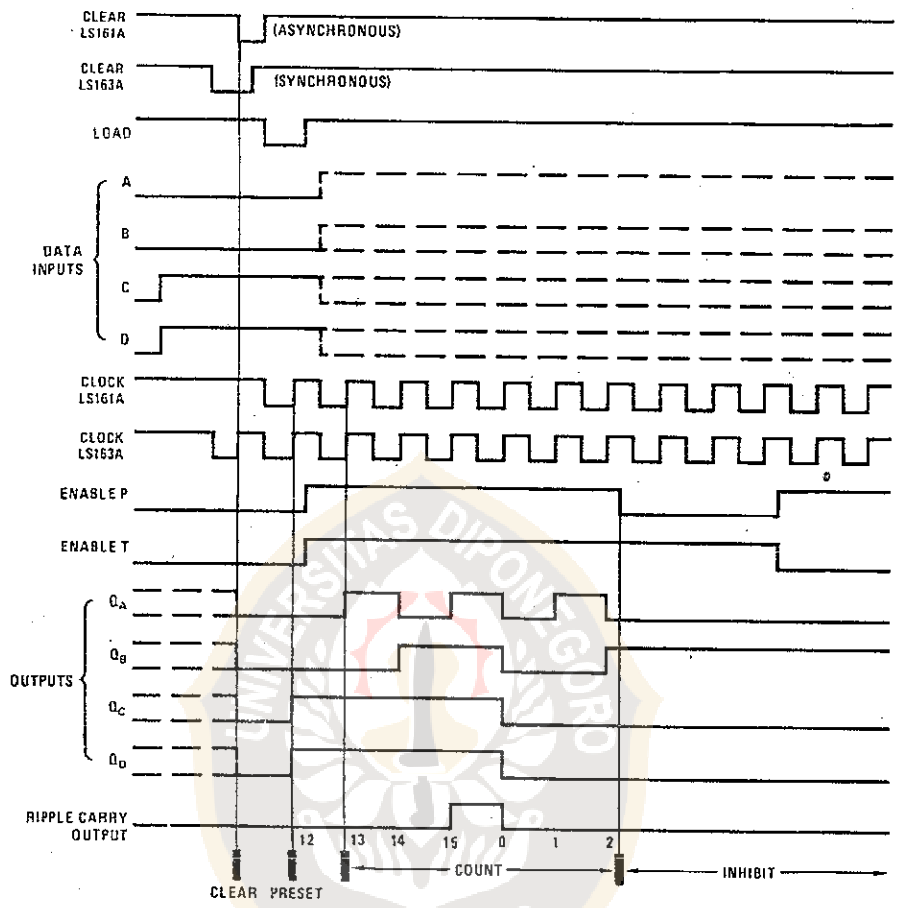
The input pulses are supplied by generators having the following characteristics:
PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_R \leq 6$ ns, $t_F \leq 6$ ns. Vary PRR to measure f_{MAX}.

Enable P and enable T setup times are measured at t_{N+0}.

$V_{REF} = 1.3V$.

Timing Diagram

LS161A, LS163A Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences



Sequence:
(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one, and two
(4) Inhibit

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DM74LS161A Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−0.4	mA
I_{OL}	LOW Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 2)		0		25	MHz
	Clock Frequency (Note 3)		0		20	MHz
t_W	Pulse Width (Note 2)	Clock	20	6		ns
		Clear	20	9		
	Pulse Width (Note 3)	Clock	25			ns
		Clear	25			
t_{SU}	Setup Time (Note 2)	Data	20	8		ns
		Enable P	25	17		
		Load	25	15		
	Setup Time (Note 3)	Data	20			ns
		Enable P	30			
		Load	30			
t_H	Hold Time (Note 2)	Data	0	−3		ns
		Others	0	−3		
	Hold Time (Note 3)	Data	5			ns
		Others	5			
t_{REL}	Clear Release Time (Note 2)		20			ns
	Clear Release Time (Note 3)		25			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 2: $C_L = 15$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5.5V$.

Note 3: $C_L = 50$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5.5V$.

DM74LS161A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = [illegible]				−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Enable T			0.2	mA
			Clock			0.2	
			Load			0.2	
			Others			0.1	
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V	Enable T			40	µA
			Clock			40	
			Load			40	
			Others			20	
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V	Enable T			−0.8	mA
			Clock			−0.8	
			Load			−0.8	
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)		−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max (Note 6)			18	31	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max (Note 7)			19	32	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CCH} is measured with the load HIGH, then again with the load LOW, with all other inputs HIGH and all outputs OPEN.

Note 7: I_{CCL} is measured with the clock input HIGH, then again with the clock input LOW, with all other inputs LOW and all outputs OPEN.

DM74LS161A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Ripple Carry		25		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Ripple Carry		30		38	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q (Load HIGH)		22		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q (Load HIGH)		27		38	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q (Load LOW)		24		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q (Load LOW)		27		38	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable T to Ripple Carry		14		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable T to Ripple Carry		15		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Any Q		28		45	ns

intel

8255A(J)
Device Characteristics

General Information	
Device Description	Programmable Peripheral
Architecture	Unavailable
Die Stepping Revision	J
Die Size	151 x 128 Mils
Number of Transistors	1,600
ESD Pass Voltage (mil-883c, m3015)	+/-1200V
Icc Typical (5v, hot c, no resistive loads)	Unavailable
Icc Max (5v, hot c, no resistive loads)	120 mA
Die Stepping Market Release Date	1286
Process Information	
Process	411
Package Information	
Designator	P
Package Type	PLASTIC DUAL-INLINE PACKAGE
Number of Leads	40
Thermal Impedance	(Theta jA) = 90.0 C/Watt (Theta jC) = 28.0 C/Watt
Package Information	
Designator	D
Package Type	CERDIP
Number of Leads	40
Thermal Impedance	(Theta jA) = 43.0 C/Watt (Theta jC) = 18.0 C/Watt

PLEASE NOTE:
This product is no longer being manufactured by Intel. THESE DOCUMENTS ARE PROVIDED FOR HISTORICAL REFERENCE PURPOSES ONLY AND ARE SUBJECT TO THE TERMS SET FORTH IN TH "LEGAL INFORMATION" LINK BELOW. For information on currently available Intel products, please see http://www.intel.com/ and/or developer.intel.com

Timer | NE/SA/SE555/SE555C

ESCRIPTION

e 555 monolithic timing circuit is a highly stable controller capable producing accurate time delays, or oscillation. In the time delay de of operation, the time is precisely controlled by one external istor and capacitor. For a stable operation as an oscillator, the e running frequency and the duty cycle are both accurately ntrolled with two external resistors and one capacitor. The circuit y be triggered and reset on falling waveforms, and the output ucture can source or sink up to 200mA.

EATURES

Turn-off time less than 2µs

Max. operating frequency greater than 500kHz

Timing from microseconds to hours

Operates in both astable and monostable modes

High output current

Adjustable duty cycle

TTL compatible

Temperature stability of 0.005% per °C

PPLICATIONS

Precision timing

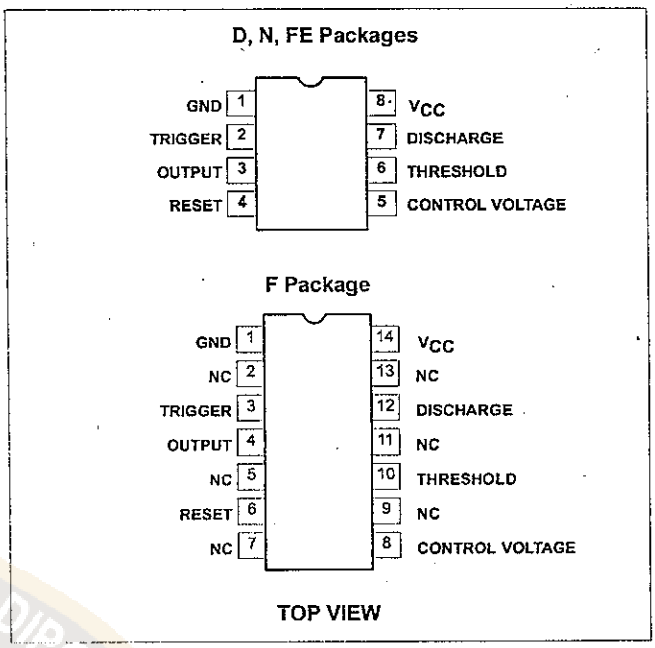
Pulse generation

Sequential timing

Time delay generation

Pulse width modulation

PIN CONFIGURATIONS



RDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE555D	0174C
-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE555N	0404B
-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA555N	0404B
-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA555D	0174C
-Pin Hermetic Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CFE	
-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555CN	0404B
4-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555N	0405B
-Pin Hermetic Cerdip	-55°C to +125°C	SE555FE	
4-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE555F	0581B
4-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555F	0581B
4-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CF	0581B

C AND AC ELECTRICAL CHARACTERISTICS

= 25°C, V_{CC} = +5V to +15 unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
			Min	Typ	Max	Min	Typ	Max	
/CC	Supply voltage		4.5		18	4.5		16	V
CC	Supply current (low state)[1]	V_{CC}=5V, R_L=∞		3	5		3	6	mA
		V_{CC}=15V, R_L=∞		10	12		10	15	mA
	Timing error (monostable)	R_A=2kΩ to 100kΩ							
M	Initial accuracy[2]	C=0.1µF		0.5	2.0		1.0	3.0	%
$\Delta t_M/\Delta T$	Drift with temperature			30	100		50	150	ppm/°C
$\Delta t_M/\Delta V_S$	Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
	Timing error (astable)	R_A, R_B=1kΩ to 100kΩ							
A	Initial accuracy[2]	C=0.1µF		4	6		5	13	%
$\Delta t_A/\Delta T$	Drift with temperature	V_{CC}=15V			500			500	ppm/°C
$\Delta t_A/\Delta V_S$	Drift with supply voltage			0.15	0.6		0.3	1	%/V
/C	Control voltage level	V_{CC}=15V	9.6	10.0	10.4	9.0	10.0	11.0	V
		V_{CC}=5V	2.9	3.33	3.8	2.6	3.33	4.0	V
/TH	Threshold voltage	V_{CC}=15V	9.4	10.0	10.6	8.8	10.0	11.2	V
		V_{CC}=5V	2.7	3.33	4.0	2.4	3.33	4.2	V
TH	Threshold current[3]			0.1	0.25		0.1	0.25	µA
/TRIG	Trigger voltage	V_{CC}=15V	4.8	5.0	5.2	4.5	5.0	5.6	V
		V_{CC}=5V	1.45	1.67	1.9	1.1	1.67	2.2	V
TRIG	Trigger current	V_{TRIG}=0V		0.5	0.9		0.5	2.0	µA
/RESET	Reset voltage[4]	V_{CC}=15V, V_{TH} =10.5V	0.3		1.0	0.3		1.0	V
RESET	Reset current	V_{RESET}=0.4V		0.1	0.4		0.1	0.4	mA
	Reset current	V_{RESET}=0V		0.4	1.0		0.4	1.5	mA
/OL	Output voltage (low)	V_{CC}=15V							
		I_{SINK}=10mA		0.1	0.15		0.1	0.25	V
		I_{SINK}=50mA		0.4	0.5		0.4	0.75	V
		I_{SINK}=100mA		2.0	2.2		2.0	2.5	V
		I_{SINK}=200mA		2.5			2.5		V
		V_{CC}=5V							
		I_{SINK}=8mA		0.1	0.25		0.3	0.4	V
		I_{SINK}=5mA		0.05	0.2		0.25	0.35	V
/OH	Output voltage (high)	V_{CC}=15V							
		I_{SOURCE}=200mA		12.5			12.5		V
		I_{SOURCE}=100mA	13.0	13.3		12.75	13.3		V
		V_{CC}=5V							
		I_{SOURCE}=100mA	3.0	3.3		2.75	3.3		V
OFF	Turn-off time[5]	V_{RESET}=V_{CC}		0.5	2.0		0.5	2.0	µs
R	Rise time of output			100	200		100	300	ns
F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA

OTES:

. Supply current when output high typically 1mA less.
. Tested at V_{CC}=5V and V_{CC}=15V.
. This will determine the max value of R_A+R_B, for 15V operation, the max total R=10MΩ, and for 5V operation, the max. total R=3.4MΩ.
. Specified with trigger input high.
. Time measured from a positive going input pulse from 0 to 0.8×V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

National Semiconductor

November 1999

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit µP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

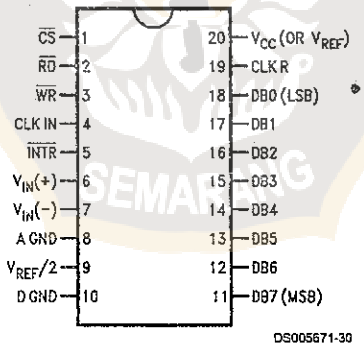
- Compatible with 8080 µP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

- Resolution 8 bits
- Total error ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time 100 µs

Connection Diagram

ADC080X
Dual-In-Line and Small Outline (SO) Packages



DS005671-30

See Ordering Information

Ordering Information

TEMP RANGE		0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	±¼ Bit Adjusted			ADC0801LCN
	±½ Bit Unadjusted	ADC0802LCWM		ADC0802LCN
	±½ Bit Adjusted			ADC0803LCN
	±1Bit Unadjusted	ADC0804LCWM	ADC0804LCN	ADC0805LCN/ADC0804LCJ
PACKAGE OUTLINE		M20B—Small Outline	N20A—Molded DIP	

Z-80® is a registered trademark of Zilog Corp.

bsolute Maximum Ratings (Notes 1, 2)

Military/Aerospace specified devices are required, ease contact the National Semiconductor Sales Office/ stributors for availability and specifications.

pply Voltage (V_{CC}) (Note 3)	6.5V
ltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC}+0.3V)
ead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0804LCJ	$-40°C \le T_A \le +85°C$
ADC0801/02/03/05LCN	$-40°C \le T_A \le +85°C$
ADC0804LCN	$0°C \le T_A \le +70°C$
ADC0802/04LCWM	$0°C \le T_A \le +70°C$
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

lectrical Characteristics

e following specifications apply for V_{CC}=5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
0802: Total Unadjusted Error (Note 8)	V_{REF}/2=2.500 V_{DC}			±½	LSB
0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
0804: Total Unadjusted Error (Note 8)	V_{REF}/2=2.500 V_{DC}			±1	LSB
0805: Total Unadjusted Error (Note 8)	V_{REF}/2-No Connection			±1	LSB
/2 Input Resistance (Pin 9)	ADC0801/02/03/05	2.5	8.0		kΩ
	ADC0804 (Note 9)	0.75	1.1		kΩ
og Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC}+0.05	V_{DC}
Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
er Supply Sensitivity	V_{CC}=5 V_{DC} ±10% Over Allowed V_{IN}(+) and V_{IN}(−) Voltage Range (Note 4)		±1/16	±⅛	LSB

C Electrical Characteristics

e following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified.

mbol	Parameter	Conditions	Min	Typ	Max	Units
	Conversion Time	f_{CLK}=640 kHz (Note 6)	103		114	µs
	Conversion Time	(Notes 5, 6)	66		73	$1/f_{CLK}$
	Clock Frequency	V_{CC}=5V, (Note 5)	100	640	1460	kHz
	Clock Duty Cycle		40		60	%
	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ =0 V_{DC}, f_{CLK}=640 kHz	8770		9708	conv/s
R)L	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ =0 V_{DC} (Note 7)	100			ns
	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L=100 pF		135	200	ns
OH	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits)		125	200	ns
RI	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
	Input Capacitance of Logic Control Inputs			5	7.5	pF

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=5.25 V_{DC}	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN}=5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN}=0 V_{DC}	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T−	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis (V_T+)−(V_T−)		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O=360 µA V_{CC}=4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O=−360 µA V_{CC}=4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 I_{OUT}=1.6 mA, V_{CC}=4.75 V_{DC} I_{OUT}=1.0 mA, V_{CC}=4.75 V_{DC}			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=−360 µA; V_{CC}=4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=−10 µA, V_{CC}=4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT}=0 V_{DC} V_{OUT}=5 V_{DC}	−3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A=25°C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A=25°C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCWM	f_{CLK}=640 kHz, $V_{REF}/2$=NC, T_A=25°C and $\overline{CS}$ =5V		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

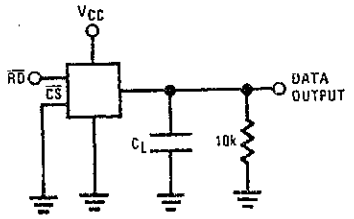
Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct–especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 4* and section 2.0.

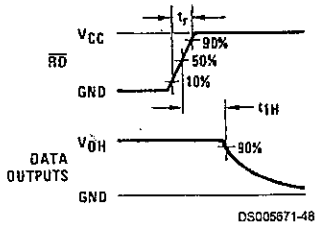
TRI-STATE Test Circuits and Waveforms

t_{1H}



DS005671-47

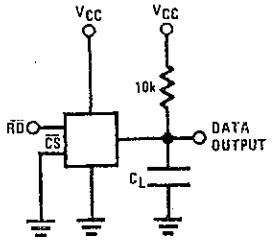
t_{1H}, C_L=10 pF



DS005671-48

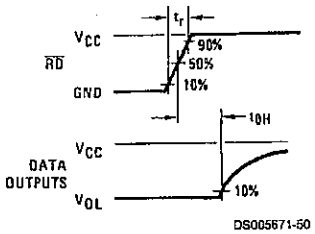
t_r=20 ns

t_{0H}



DS005671-49

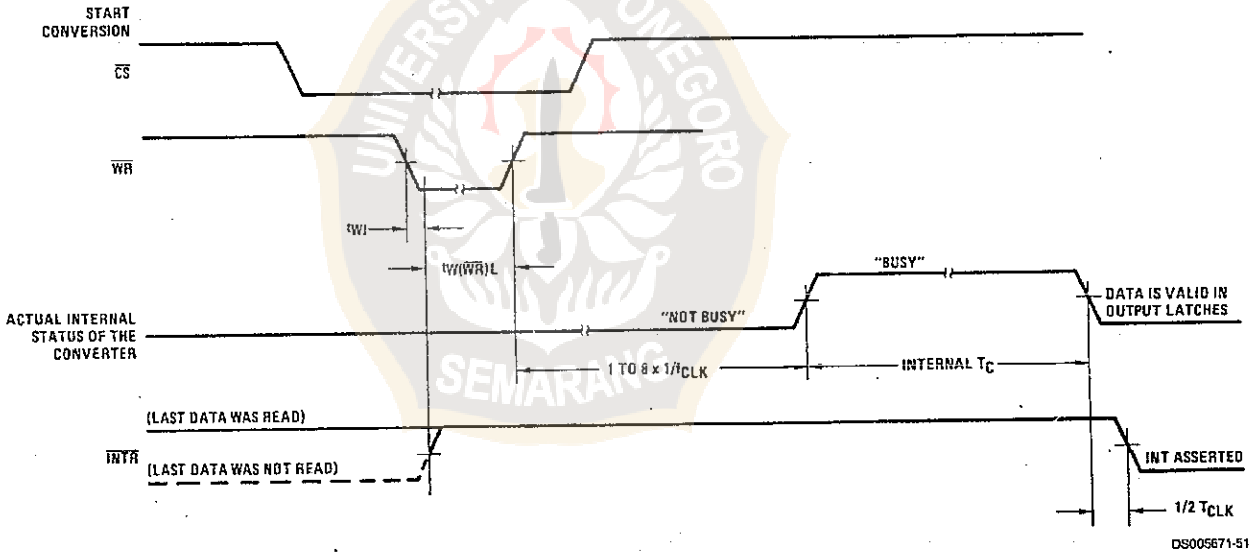
t_{0H}, C_L=10 pF



DS005671-50

t_r=20 ns

Timing Diagrams (All timing is measured from the 50% voltage points)



DS005671-51